



A COMPARATIVE STUDY ON TUNNEL FET AND DOPINGLESS TUNNEL FET

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ABSTRACT

In today's world nm technology plays a major role. In this nano world along with application of scaling down of the devices there are many challenges that are faced due to the reduction in sizes. DLTFET's are one type of nano FET'S which are able to face some of the challenges efficiently. DLTFET's are able to reduce the high temperature requirements of conventional TFET'S. They are also able to achieve to a lower sub threshold swing. In DLTFET's rather than the forming the source and drain using high temperature annealing techniques, they are formed using charge plasma concepts. Due to this new techniques RDF'S can be avoided in DLTFET's. In this paper we are going to present a comparative study on TFET and types of DLTFET.

Key words: TFET, DLTFET, DODLTFET, HGDODLTFET, MLTFET, SCE, BTBT, RDF, SS_{av}, ION/IOFF, V_{th}.

I. INTRODUCTION

To enhance the performance of MOS device scaling down the sizes is rapid in recent times. Scaling down of the sizes of MOS devices increases the speed and packing density. It reduces the power consumption and also the chip cost. In addition to the above advantages some of the challenges are also to be faced. When the devices are scaled down leakage current increases followed by the static power dissipation [15]. When the device is scaled down the power supply also should be scaled down which in turn degrades the ON- state performance of the device. These are some of the challenges faced by the scaled down MOS device. Also the sub threshold slope of MOS device is limited to 60mv/decade. To overcome these challenges rather conventional MOS devices TFET'S are having more advantages. TFET's are the devices which work with respect to the BTBT process rather than the thermionic emission of the charge carriers. These TFET's have come into play because of their sub threshold slope which can be less than 60mv/decades which is steep [17][21]. The impact of short channel effects is less. TFET's are known for their performance at low power. However these TFET's too have disadvantages of poor on current, SCE's [9] and also the effect of random dopant fluctuations [11]. Also for efficient tunneling mechanism to occur abrupt junctions are necessary but formation of abrupt junctions using high thermal annealing processes is difficult.

To answer the challenges faced by TFET's more efficiently doping less TFET's has come into picture. A doping less TFET is formed without the use of any high thermal energy requirement. The formation of source and drain is due to charge plasma concept, on a intrinsic silicon by the use of metal electrodes with appropriate work functions[1]. A charge plasma diode and charge plasma transistor has already come into existence [12-13]. In the construction of DLTFT high temperature requirements are avoided, hence the effect of RDF's is less. Also in DLTFT's care must be taken to maintain the silicon wafer thickness has 10 nm to avoid quantum mechanical effects [14]. DLTFT's can have improved on state performance. As the high temperature requirements are avoided, abrupt junctions can be formed which in turn increases the tunneling efficiency and also the on-state current of the device. With the usage of high k dielectric at the gate also the on state current can be improved which in turn increases the I_{ON}/I_{OFF} ratio the frequency of operations of a normal MOSFET is almost 200 KHz and for a TFET the operating frequency is 200KHz but for a DLTFT it is 8Ghz comparatively. In DLTFT's also the performance can be improved in different ways. The on current can be controlled efficiently in a DGDLTFT. Using different oxide materials under source and drain i.e. a DODGDLTFT also the performance can be enhanced by reducing the SS_{av} to a still lower level. Also there is another type called MLDLTFT which uses a layer of metal in the oxide layer which is in between gate and source. For DODLTFT AND HGDODLTFT the frequencies of operation are 42.5 GHz and 103 GHz respectively. All these types of DLTFT's have their own advantages with trade of between some of the parameters. But at lost without degrading the performance of TFET's the DLTFT's are able to give good parameters compared to TFET's in this paper we are going to present the comparison between TFET and DLTFT's based on the study made on different papers.

II. CONSTRUCTION

In the construction of TFET source and drain are formed by the conventional method of doping the impurities which requires very high temperatures. Fig (1) shows the schematic and band diagrams of n-channel TFET. This can be overcome by using other type of FET called DLTFT (doping less TFET) in which the source and drain regions are formed by charge plasma concept.

In DLTFT the source and drain are formed by inducing metal electrodes with suitable work functions. Figure 2 shows the cross sectional view of a double gate doping less TFET. Normal TEFT has less BTBT efficiency because of absence of abrupt functions. When source and drain are formed by doping method then formation of abrupt function is not possible. In DLTFT tunneling faced by conventional TFET's is that due to usage of expensive thermal annealing techniques they are affected by RDF. They show effect on the off state performance of the device by increasing the leaking current. These RDF's can be reduced to some extent in DLTFT due to their avoidance of doping techniques. From the above construction features it is obvious that DLTFT has more advantages than conventional TFET. A DODLTFT uses a high K gate dielectric on the source side which results in the further reduction of the tunneling width and improvement in the ON current compared to DLTFT. Figure 3 shows the schematic of DODLTFT employing different oxide materials below source and drain. Under

the gate the dielectric layer is occupied by both the oxides equally. As in the figure 4 showing the schematic of HGDODLTFET it employs a metal of low work function on the top of tunneling junction and also a high K dielectric on the source side which improves the ON state performance of the device [6]. From figures 9, 10 showing the energy band diagrams and the transfer characteristics of the HG-DO-DLTFET it is observed that the device has better performance than the normal DLTFET [16][20]. The schematic of ML-TFET is shown in figure 5. In a MLTFET the band steepness at the source channel interface is improved due to the presence of metal layer in the oxide region between the gate and source electrodes. This reduces the tunneling barrier and I_{on} , SS & V_{th} are improved. Figures 11 and 12 show the energy band diagrams and the transfer curve of the ML-TFET. The presence of the metal layer enhances the tunneling rate and hence the switching rate of a ML-TFET is high.

III. WORKING

The figure 6 shows the energy band diagrams of TFET and DLTFET. The threshold voltage was found to be 0.12V which is almost similar for both the devices. Both are almost similar. In the off state condition conduction band edge of the source is above the valence band edge of the channel which makes no space for tunneling. Hence off state current is less. When the device is on, since TFET is operated in reverse bias, the source is grounded and positive voltage is applied across the drain. If the gate voltage is zero again there is no current through the device as the gate voltage increases tunneling width decreases and a high ON current flows through the device. The working of DLTFET is similar to that of TFET. Either in TFET or DLTFET if dual gate is used then the gate potential can be more efficiently controlled [10][19]. Hence it can be seen that without compromise in any of the features i.e. in working or construction, the DLTFET can be viewed as an improved TFET with avoiding the high temperature requirements although it has the same SS and I_{on}/I_{off} ratio as that of conventional TFET.

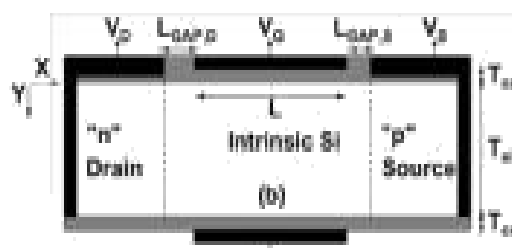


Fig.1 Cross sectional view of the double gate doping-less TFET.

Figure 7 shows the energy band diagram of DODLTFET. In both DL-TFET and DO-DL-TFET the conduction band energy levels of channel are aligned with valence band energy levels of source side, but because of the use of high -k dielectric material on the source side the tunneling width is less in the DODLTFET compared to the normal DLTFET. From the figure 8 the transfer characteristics of DODLTFET compared to that of DL-TFET it can be observed that for a DGDODLTFET the ON current is improved and also it has a steeper sub-threshold slope and improved I_{on}/I_{off} ratio[20].

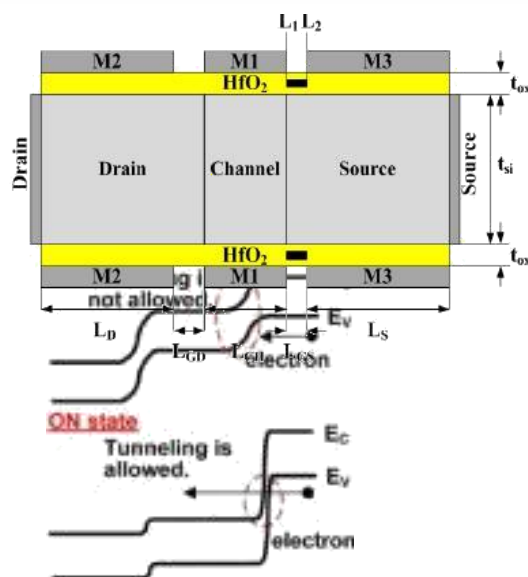


Fig. 2 Device schematic and band diagram in the ON/OFF states of the n-channel TFET.

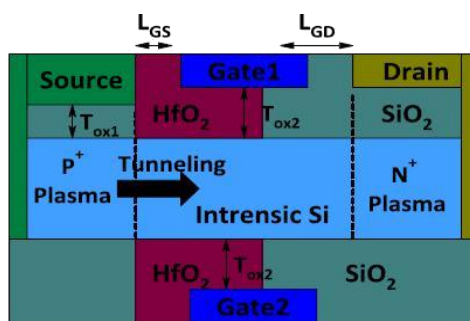


Fig3: Schematic diagram of DG-DO-DL-TFET

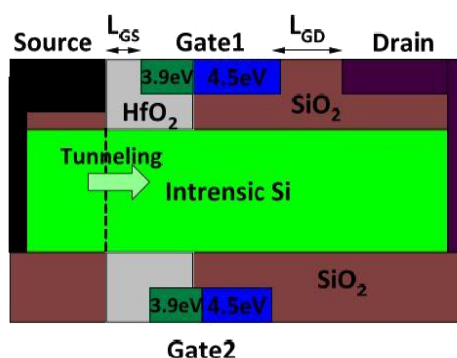


Fig4: Schematics of HG-DLTFET

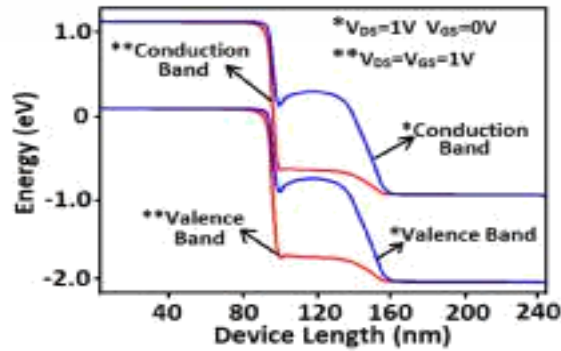


Fig5 : Schematics of ML-DLTFET

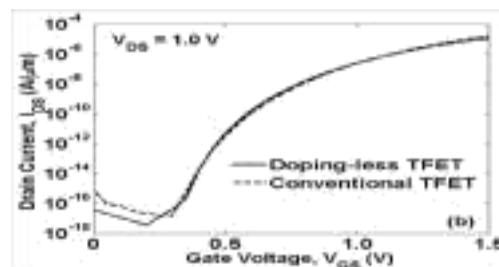


Fig. 6: Transfer characteristics of the doping-less TFET compared with that of the corresponding conventional TFET for $V_{DS} = 1.0 V$

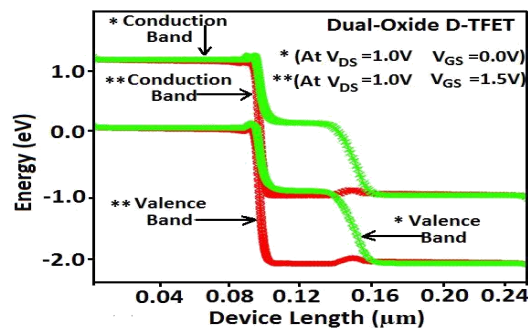


Fig7 : Energy band diagram of DO-DG-DL-TFET under thermal nonequilibrium and ON-state conditions

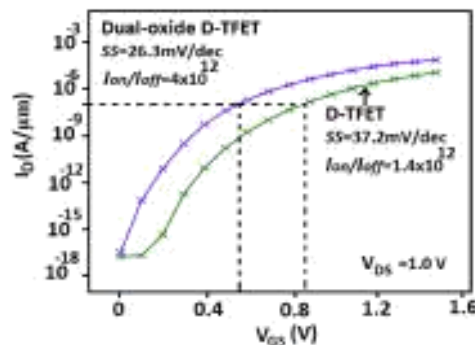


Fig8: Transfer characteristics of the Proposed DG-DO-DL-TFET

Fig. 9: Band diagrams of HGDL-TFET in the OFF-state ($V_{GS} = 0V$, $V_{DS} = 1.0 V$) and in ON-state ($V_{GS} = V_{DS} = 1.0 V$) conditions.

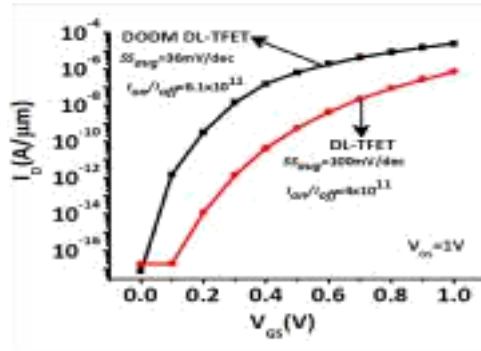


Fig. 10: Transfer characteristics of DL-TFET and the HG-DL-TFET devices.

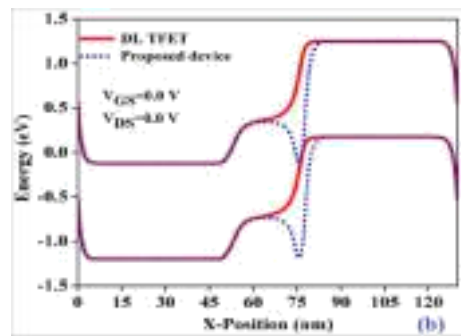


Fig. 11: Variation of energy band along the channel direction in thermal equilibrium state for ML-TFET

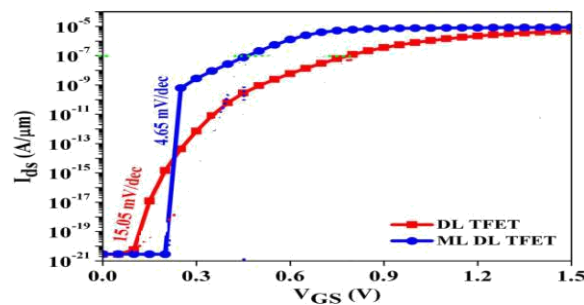


Fig. 12: Transfer characteristics of ML-TFET and the DL-TFET devices.

IV. PARAMETRES WISE 4.1 Sub threshold swing

MOSFET'S are limited off to a SS of 60mv/decade. Coming to TFET they have SS less than 60mv/decade approximately of 52.8 mV/decade at room temperature[2], where as in a normal DLTFET it is 100mV/decade[1]. As it is the introductory device, it has this disadvantage but in its constructions high temperatures are not required. In a DODLTFET 30% improvement is achieved in SS[3] where as in a HGDO



DLTFET there is a 3.8% of improvement which is 37mv/decade and for a ML DLTFET SS is as less as possible which is 5 mV/decade compared to all the above devices.

4.2. ON CURRENT

The ON current of TEFT is approximately 1 μ A per μ m. The on current can be further improved by use of lower band gap material, lower oxide thickness and more abrupt source doping profile. The DLTFET has the ON current as -1.1×10^{-5} A/ μ m which is almost similar to that of the conventional TFET. A DODLTFET improves the ON current nearly 6.14 times than the DLTFET. In a HGDODLTFET [4] the combination of low work function metal and high K dielectric gives an improved ON state performance and the ON current is increased by 65 times compared to the DLTFET. Due to the band steepness in a MLTFET the switching speed increases[5].

4.3 Ion/Ioff RATIO

The ON and OFF currents of TFET are 12.1a and 5.4a per micrometer at a Vgs of 1v. Even though TFET has less

SS value its Ion/Ioff ratio is less than the conventional MOSFET'S. The Ion/Ioff ratio of DL-TFET is also similar to that of a TFET except the advantage of having no requirement of high temperatures at the time of construction. In a DODLTFET and HG-DLTFET the Ion/Ioff ratio is enhanced by 6.14 and 74 times respectively compared to DLTFET.

V. APPLICATIONS

Due to the ambipolar behavior of the TFET it can be used in BIOSENSING applications [7]. Also TFET can be used as energy efficient electronic switch [18] and as a memory device[8]. DLTFET's are relevant for low power applications.

VI. CONCLUSION

This paper is a comparative study between the conventional TFET and different types of Doping less TFET's. From the study it has been observed that compared to a conventional TFET all the DLTFET's which have been taken into consideration have improved performance in terms of I_{on} , I_{on}/I_{off} ratio, threshold voltage, frequency of operation. Furthermore it can be seen that an MLTFET shows a good performance with a high switching speed compared to others. From this paper it can be easily said that the challenges faced by TFET can be overcome by DLTFET's.

VII. FUTURESCOPE

DLTFET's with their improved characteristics are attracting the researchers and VLSI industry. They provide a new way into the future of low power applications, with their high ON CURRENT, better control on channel width, improved threshold voltage and reduction of thermal budget. With all these advantages DLTFET'S may rule the VLSI area in future.



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