Volume No.06, Issue No. 11, November 2017 www.ijarse.com



HIGH STEP-UP DC/DC CONVERTER BASED ON SWITCHED-CAPACITOR TECHNIQUES FOR RENEWABLE ENERGY APPLICATIONS

G.Divyasree¹, M.Sreelekha², T.Chaitanya³

ABSTRACT

In this paper, a novel high step-up dc/dc converter is presented for renewable energy applications. The suggested structure consists of a coupled inductor and two voltage multiplier cells, in order to obtain high step-up voltage gain. In addition, two capacitors are charged during the switch-off period, using the energy stored in the coupled inductor which increases the voltage transfer gain. The energy stored in the leakage inductance is recycled with the use of a passive clamp circuit. The voltage stress on the main power switch is also reduced in the proposed topology. Therefore, a main power switch with low resistance $R_{DS(ON)}$ can be used to reduce the conduction losses. The operation principle and the steady-state analyses are discussed thoroughly.

Index Terms—Coupled inductor, dc/dc converters, high step-up, switched capacitor.

I. INTRODUCTION

Demand for clean and sustainable energy sources has dramatically increased during the past few years with growing population and industrial development. For a long time, fossil fuels have been used as the major source of generating electrical energy. Environmental consequences of these resources have made it necessary to benefit from clean energy sources such as wind and solar. Therefore, distributed generation (DG) systems based on renewable energy sources have attracted the researchers' attention. The DG systems include photovoltaic (PV) cells, fuel cells and wind power [1]–[3]. However, the output voltages of these sources are not large enough for connecting to ac utility voltage. PV cells can be connected in series in order to obtain a large dc voltage. However, it is difficult to ignore the shadow effect in the PV panels [4]–[6]. High step-up converters are a suitable solution for the aforementioned problem. Each PV panel can be connected to a particular high step-up converter. Therefore, each panel can be controlled independently. These converters boost the low-input voltages (24–40 V) to a high-voltage level (300–400 V) [7]. The main features of high step-up converters are their large conversion ratio, high efficiency, and small size [8]–[10]. Theoretically, conventional boost converters can achieve high-voltage gain with an extremely high duty ratio [11].

However, the performance of the system will be deteriorated with a high duty cycle due to several problems such as low conversion efficiency, reverse-recovery, and electromagnetic interference problems [12]. Some transformer-based converters like forward, push–pull, or flyback converters can achieve high step-up voltage gain by adjusting the turn ratio of the transformer. However, the leakage inductor of the transformer will cause serious problems such as voltage spike on the main switch and high power dissipation [13]. In order to improve

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the conversion efficiency and obtain high step-up voltage gain, many converter structures have been presented [14]. Switched capacitor [14] and voltage lift techniques have been used widely to achieve high step-up voltage gain. However, in these structures, high charging currents will flow through the main switch and increase the conduction losses. Coupled-inductor-based converters can also achieve high step-up voltage gain by adjusting the turn ratios. However, the energy stored in the leakage inductor causes a voltage spike on the main switch and deteriorates the conversion efficiency. To overcome this problem, coupled-inductor-based converters with an active-clamp circuit have been presented. Some high step-up converters with two-switch and single-switch are introduced in the recent published literatures. However, the conversion ratio is not large enough. This paper presents a novel high step-up dc/dc converter for renewable energy applications. The suggested structure consists of a coupled inductor and two voltage multiplier cells in order to obtain high-step-up voltage gain. In addition, a capacitor is charged during the switch-off period using the energy stored in the coupled inductor, which increases the voltage transfer gain. The energy stored in the leakage inductance is recycled with the use of a passive clamp circuit. The voltage stress on the main power switch is also reduced in the proposed topology. Therefore, a main power switch with low resistance RDS(ON) can be used to reduce the conduction losses. The

operation principle and the steady-state analyses are discussed thoroughly. To verify the performance of the presented converter, a 300-W laboratory prototype circuit is implemented. The results validate the theoretical

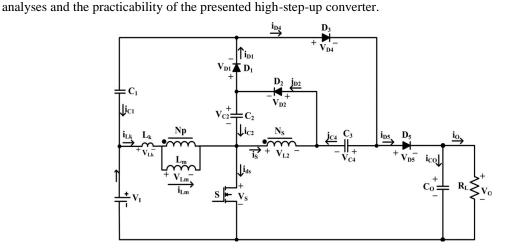


Fig. 1. Circuit configuration of the presented high-step-up converter.

II. OPERATING PRINCIPLE OF THE PROPOSED CONVERTER

The circuit configuration of the proposed converter is shown in Fig. 1. The proposed converter comprises a dc input voltage (VI), active power switch (S), coupled inductor, four diodes, and four capacitors. Capacitor C1 and diode D1 are employed as clamp circuit respectively. The capacitor C3 is employed as the capacitor of the extended voltage multiplier cell. The capacitor C2 and diode D2 are the circuit elements of the voltage multiplier which increase the voltage of clamping capacitor C1. The coupled inductor is modeled as an ideal transformer with a turn ratio N (NP/NS), a magnetizing inductor Lm and leakage inductor Lk. In order to simplify the circuit analysis of the converter, some assumptions are considered as follows:

IJARSE

ISSN: 2319-8354

Volume No.06, Issue No. 11, November 2017 www.ijarse.com

- IJARSE ISSN: 2319-8354
- 1) All Capacitors are sufficiently large; therefore VC1, VC2, VC3, and VO are considered to be constant during one switching period;
- 2) All components are ideal but the leakage inductance of the coupled inductor is considered. According to the aforementioned assumptions, the continuous conduction mode (CCM) operation of the proposed converter includes five intervals in one switching period. The current-flow path of the proposed converter for each stage is depicted in Fig. 2. Some typical waveforms under CCM operation are illustrated in Fig. 3. The operating stages are explained as follows.

Stage I [t0 < t < t1 see Fig. 2(a)]: In this stage, switch S is turned ON. Also, diodes D2 and D4 are turned ON and diodes D1 and D3 are turned OFF. The dc source (VI) magnetizes Lm through S. The secondary-side of the coupled inductor is in parallel with capacitor C2 using diode D2. As the current of the leakage inductor Lk increases linearly, the secondary side current of the coupled inductor (iS) decreases linearly. The required energy of load (R) is supplied by the output capacitor CO. This interval ends when the secondary-side current of the coupled inductor becomes zero at t = t1.

Stage II [t1 < t < t2 see Fig. 2(b)]: In this stage, switch S and diode D3 are turned ON and diodes D1, D2, and D4 are turned OFF. The dc source VI magnetizes Lm through switch S. So, the current of the leakage inductor Lk and magnetizing inductor Lm increase linearly. The capacitor C3 is charged by dc source VI, clamp capacitor and the secondary-side of the coupled inductor. Output capacitor CO supplies the demanded energy of the load RL. This interval ends when switch (S) is turned OFF at t = t2.

Stage III [t2 < t < t3 see Fig. 2(c)]: In this stage, switch S is turned OFF. Diodes D1 and D3 are turned ON and diodes D2 and D4 are turned OFF. The clamp capacitor C1 is charged by the stored energy in capacitor C2 and the energies of leakage inductor Lk and magnetizing inductor Lm. The currents of the secondary-side of the coupled inductor (iS) and the leakage inductor are increased and decreased, respectively. The capacitor C3 is still charged through D3. Output capacitor C3 supplies the energy to load RL. This interval ends when iLk is equal to iLm at t = t3.

Stage IV [t3 < t < t4 see Fig. 2(d)]: In this stage, S is turned OFF. Diodes D1 and D4 are turned ON and diodes D2 and D3 are turned OFF. The clamp capacitor C1 is charged by the capacitor C2 and the energies of leakage inductor Lk and magnetizing inductor Lm. The currents of the leakage inductor Lk and magnetizing inductor Lm decrease linearly. Also, a part of the energy stored in Lm is transferred to the secondary side of the coupled inductor. The dc source VI, capacitor C3 and both sides of the coupled inductor charge output capacitor and provide energy to the load RL. This interval ends when diode D1 is turned OFF at t = t4.

Stage V [t4 < t < t5 see Fig. 2(e)]: In this stage, S is turned OFF. Diodes D2 and D4 are turned ON and diodes D1 and D3 are turned OFF. The currents of the leakage inductor Lk and magnetizing inductor Lm decrease

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linearly. Apart of stored energy in Lm is transferred to the secondary side of the coupled inductor in order to charge the capacitor C2 through diode D2. In this interval the dc input voltage VI and stored energy in the capacitor C3 and inductances of both sides of the coupled inductor charge the output capacitor C3 and provide the demand energy of the load RL. This interval ends when switch S is turned S is turned S is turned S.

III. STEADY-STATE ANALYSIS OF THE PROPOSED CONVERTER

3.1 CCM Operation

To simplify the steady-state analysis, only stages II, IV, and V are considered since these stages are sufficiently large in comparison with stages I and III. During stage II, Lk and Lm are charged by dc source VI.

Therefore, the following equation can be written according to Fig. 2(b):

$$V_{Lm} = kV_1 \tag{1}$$

Where k is the coupling coefficient of coupled inductor, which equals to Lm/(Lm + Lk). Capacitor C3 is charged by clamp capacitor C1, dc source (VI), and the secondary-side of the coupled inductor. The voltage across the capacitor C3 can be expressed by

$$V_{c3} = V_{c1} + (kn + 1)V_1 \tag{2}$$

Where n is the turn ratio of coupled inductor which is equal to NS/N. As shown in Fig. 2(d), during stage IV, Lk and Lm demagnetize to the clamp capacitor C1 with the help of capacitor C2. Hence, the voltage across Lm can be written as

$$V_{Lm} = k(V_{c2} - V_{c1}) (3)$$

Also, the output voltage can be formulated based on Fig. 2(d)

$$V_0 = V_1 + V_{c3} + (kn + 1)(V_{c1} - V_{c2})$$
(4)

According to Fig. 2(e), in the time interval of stage V, the voltage across Lm can be expressed by

$$V_{Lm} = \frac{v_{c2}}{n} \tag{5}$$

Moreover, the output voltage is derived as

$$V_o = V_1 + V_{c2} + \left(\frac{1}{kn} + 1\right)$$
 (6)

According to aforementioned assumption, the output capacitor voltage is constant during one switching period. Therefore, by equalization of (4) and (6), the following equation is derived as:

$$V_{c1} = \frac{kn+1}{kn} V_{c2}$$
 (7)

Using the volt-second balance principle on Lm and equations (1), (3), (5) and (7), the voltages across capacitors C1 and C2 is obtained as

$$V_{c1} = \frac{(kn+1)D}{1-D} V_1 \tag{8}$$

$$V_{c1} = \frac{knD}{1-D} V_1 \tag{9}$$

Substituting (8) into (2), yields

$$V_{c2} = \frac{knD}{1-D} V_1$$

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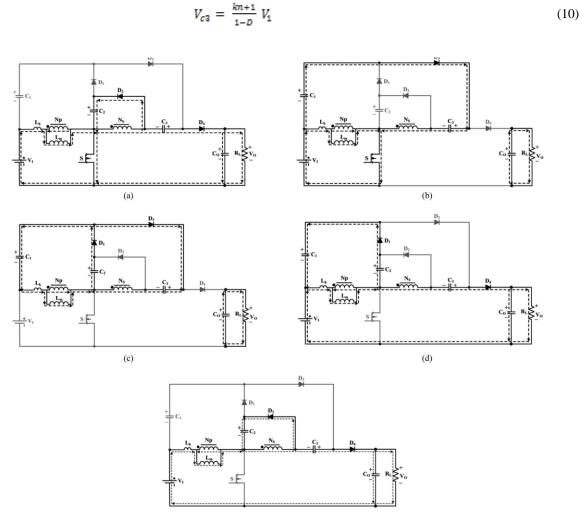


Fig. 2. Current-flow path of operating modes during one switching period at CCM operation. (a) Mode I. (b) Mode II. (c) Mode IV. (e) Mode V.

Substituting (9) and (10) into (6), the voltage gain is achieved as

$$M_{CCM} = \frac{2 + kn + knD}{1 - D} V_{1}$$

$$M_{CCM}$$

$$\begin{array}{c} & & & \\$$

Fig. 3. Voltage gain versus duty ratio under various coupling coefficients of the coupled inductor.

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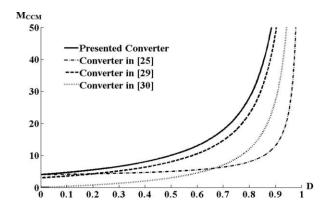


Fig. 4. Voltage gain versus duty ratio of the proposed converter, the converters at CCM.

When k equals 1, the ideal voltage gain is obtained as

$$M_{ccm} = \frac{2+n+nD}{1-D} V_1 \tag{12}$$

The voltage gain versus duty ratio of the proposed converter and the converters proposed under CCM operation with k = 1 and n = 2 are depicted in Fig. 3. As it is shown n Fig. 4 the proposed converter has higher voltage transfer gain in comparison with other converters. Also, the voltage transfer gain of the presented converter is higher than the converter presented. However, in comparison with the presented converter, an additional diode, an extra capacitor, and a multiwinding coupled inductor is utilized in the converter presented. Based on the description of the operating modes, the voltage stresses on the active switch S and diodes D1, D2, D3, and D4 are expressed as

$$V_{Ds} = V_{D1} = \frac{1}{1-D}V_1 = \frac{1}{2+2n}(V_0 + nV_1)$$
 (13)

$$V_{D2} = \frac{n}{1-D} V_1 = \frac{n}{2+2n} (V_0 + nV_1)$$
 (14)

$$V_{D3} = V_{D4} = \frac{1+n}{1-D}V_1 = \frac{1}{2}(V_0 + nV_I)$$
 (15)

According to Fig. 2, the average value of input current can be achieved as follows when switch is turned on/off:

$$I_{in(nn)} = (n+1)I_{nn} + I_{lm} (16)$$

$$I_{in(off)} = I_o (17)$$

From (16) and (17), the average current value of magnetizing inductor can be obtained as follows:

$$I_{Lm} = \frac{(M_{ccm} - 2 - n)I_o}{D} = \frac{2(n+1)}{1 - D} I_o$$
 (18)

The integral form of the current equation of magnetizing inductor can be written as

$$i_{Lm}(t) = i_{Lm}(t_o) + \frac{1}{L_m} \int_{to}^{t} v_{Lm}(T) dT$$
 (19)

Substituting (16) into (19), and for k = 1, t = DT, and t0 = 0, yields



 $\Delta i_{Lm} = \frac{DV_{in}}{L_{m}f_{c}} \tag{20}$

ISSN: 2319-8354

Applying the ampere–second balance principle on capacitors, the average current values of diodes are equal to *IO*. Therefore, the peak values of diodes *D*3 and *D*4 can be obtained as

$$i_{DS(peak)} = \frac{2I_o}{D} \tag{21}$$

$$i_{D4(peak)} = \frac{2I_o}{1-D}$$
 (22)

$$i_{s(peak)} = i_{D1(peak)} = \left(\frac{2+n+nD}{D(1-D)}\right) I_o + \frac{DV_{in}}{L_{m}f_s}$$
 (23)

Neglecting modes I and III, the time interval of modes IV and V are given as

$$d_4 = \frac{2I_o}{i_{D1(peak)}} = \frac{1-D}{n+1} \tag{24}$$

$$1-D-d_4 = d_5 (25)$$

From equation (25), the peak value of diode D2 is obtained as

$$i_{D2(peak)} = \frac{2(n+1)I_0}{n(1-D)}$$
 (26)

3.2 Boundary Conduction Mode (BCM) Operation

Similar to the analysis done in the former section, the voltage conversion ratio of the presented converter in discontinuous conduction mode (DCM) can be obtained as follows:

$$M_{DCM} = \frac{V_o}{V_A} = \frac{n+2+\sqrt{(n+2)^2 + \frac{D^2}{\pi L_m}}}{2}$$
 (27)

If the proposed converter is operated in BCM, the voltage gain in the CCM will be equal to its voltage gain in the DCM operation. From (12) and (27), the boundary normalized magnetizing inductor time constant τLmB can be formulated as

$$\tau L_{m,B} = \frac{D(1-D)^2}{8(n^2(1+D)+n(3+D)+1)}$$
 (28)

The normalized magnetizing-inductor time constant τLm can be written as

$$\tau L_m = \frac{f_s L_m}{R_L} \tag{29}$$

Fig. 6 shows the curve of τLmB . If τLm is larger than τLmB , the proposed converter is operated under CCM. Fig. 7 shows the comparison of τLmB of the presented converter with converters with respect to the duty cycle and the conversion ratio. As it is shown in Fig. 5, the CCM region of the presented converter is wider. Also, the CCM region of the presented converter is wider than the converter presented. Therefore, the presented converter requires a smaller magnetizing inductance to assure the CCM operation of the converter.

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IV. CAPACITORS AND INDUCTANCE CALCULATION

The magnetizing inductance of the coupled inductor is designed according to (28) and (29). To assure the CCM operation of the presented converter, the value of τLm must be more than $\tau Lm,B$. Therefore, the minimum value of the magnetizing inductance can be calculated as follows:

$$L_{m \ min} = \frac{D(1-D)^2 R_L}{8 f_s(n^2(1+D) + n(3+D) + 1)}$$
(30)

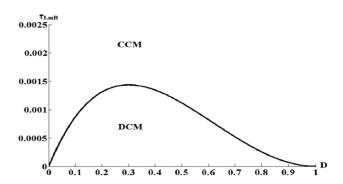


Fig.5. Boundary condition of the proposed converter under n = 2.

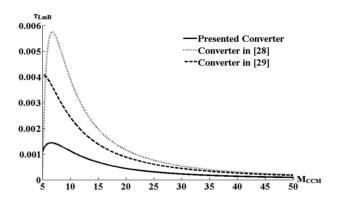


Fig. 6. Comparison of τLmB of the presented converter with converters. (a) τLmB with respect to the duty cycle. (b) τLmB with respect to the conversion ratio

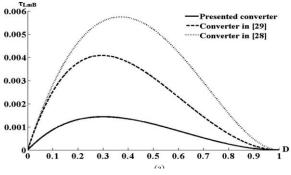


Fig. 7. Comparison of τLmB of the presented converter with converters. (a) τLmB with respect to the duty cycle. (b) τLmB with respect to the conversion ratio

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According to (30), the magnetizing inductance should be more than 148 μ H. A coupled inductor with the magnetizing inductance of the 300 μ H is employed to guarantee the CCM operation of the implemented converter. In order to design the size of the capacitors, it should be followed four conditions regarding the ripple in the output voltage. The conditions are ripple of the capacitor current, ripple due to the equivalent series resistance (ESR) of the capacitor, ripple due to the equivalent series inductance (ESL) of the capacitor, and the hold-up time requirement for load step response which the last condition is for the output capacitor. First, the design is started by considering only the first condition which ESRs and ESLs are not known before selecting the capacitor.

Specifications	Vales
Input dc voltge	V _{in} =40V
Output dc voltage	V _{out} =400V
Switching frequency	F=60KHz
Fast Diodes D ₁ , D ₂ ,D ₃ , D ₄	U1560
Coupled inductor	L _K :1μH, L _m : 300 μH
Capacitors C_1 , C_2 , C_3 , C_0 ,	47, 47,100,220 μ F
Load	300W
Power Switch(MOSFET)	IRFP260

TABLE-I Simulation Specifications

V. SIMULATION RESULTS

The performance of the converter is assessed using the circuit implemented in the MATLAB software. The specifications of the implemented circuit are given in Table I.

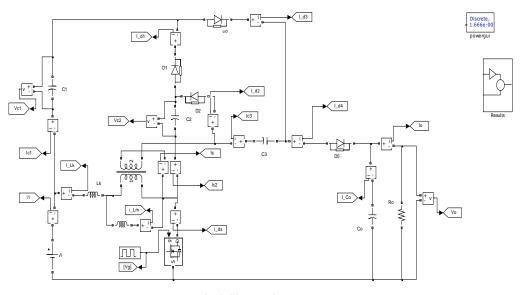


Fig.8 Simulation model





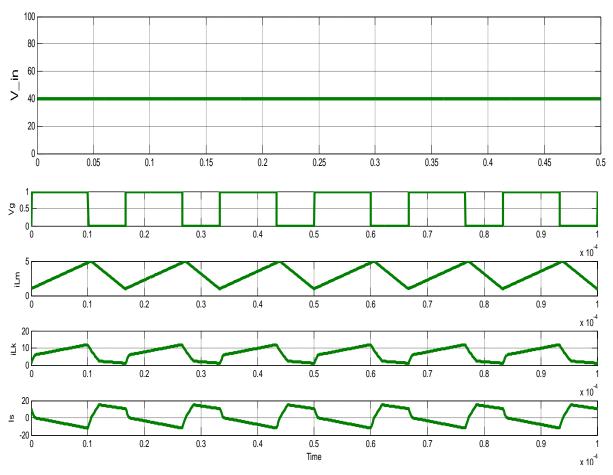


Fig. 9 Simulation results for Input voltage, Vg, iLm, iLk iLk and Is

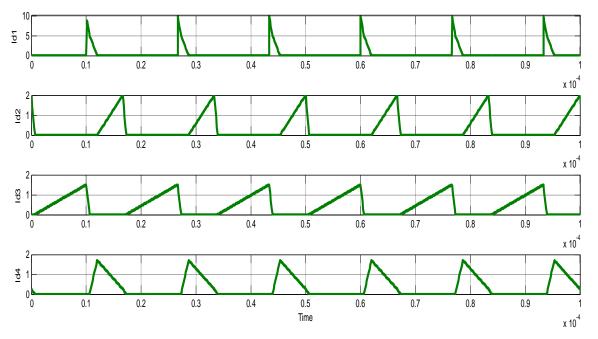


Fig. 10 Simulation results for Id1, Id2, Id3 and Id4

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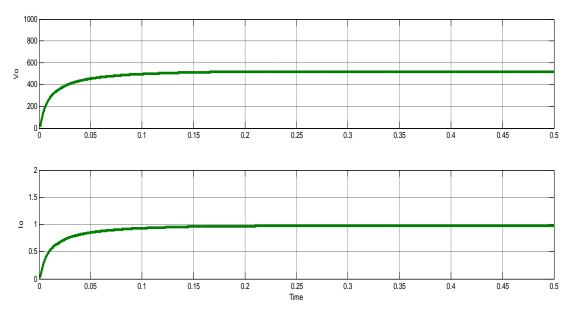


Fig. 11 Simulation results for output voltage and output current

The simulation results are shown in Fig. 9 under load 300 W. The results verify the analysis of the steady-state operation. The voltage on the switch (*V*DS) during the turn-off state is clamped to about 80 V. Therefore, a low-voltage-rated switch can be used to improve the efficiency of the converter. The Simulation model is shown in figure 8.

Simulation results for output voltage and output current is shown in figure 11. Fig. 9 shows that the energy stored in the leakage inductance is recycled to capacitor *C*1 through diode *D*1. Fig. 9 depicts the voltage stresses on the main switch and diodes. Also, shows the voltages on capacitors *C*1, *C*2, *C*3, and *C*O, which are in consistency with. The current waveforms of the diodes, switches, and the coupled inductor (*i*LK) shown in Fig. 9 validate the analysis and the feasibility of the converter. The Diode D1, D2, D3 and D4 current waveforms are shown in figure 10. The input current ripple is as much as other high-step-up converters such as the converters. However, as it is shown in Fig. 9 (*i*Source), a low-pass filter can be used to reduce the input current ripple.

VI. CONCLUSION

This paper presents a new high-step-up dc/dc converter for renewable energy applications. The suggested converter is suitable for DG systems based on renewable energy sources, which require high-step-up voltage transfer gain. The energy stored in the leakage inductance is recycled to improve the performance of the presented converter. Furthermore, voltage stress on the main power switch is reduced. Therefore, a switch with a low on-state resistance can be chosen. The steady-state operation of the converter has been analyzed in detail. Also, the boundary condition has been obtained. Finally, a hardware prototype is implemented which converts the 40-V input voltage into 400-V output voltage. The results prove the feasibility of the presented converter.

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