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A Competent RRC Interpolation Reconfigurable Filter for Wireless Communications

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ABSTRACT

The thought of designing a reconfigurable architecture has become absolutely necessary and challenging task for designers in this world to provide multistandard wireless communication. For this we proposes a reconfigurable FIR filter design with more than one interpolation and roll-off factors to support heterogeneous modern wireless communication principles. Furthermore, the planned filter presents good and great operating frequency with less area and delay. On the other hand, this paper also proposes the principal element of any filter, i.e, a constant multiplier using 2-bit (BCSE) algorithm. This proficient multiplication unit gives good improvement in the product of area and delay compare with earlier works. Moreover, the projected design is a multiplexer-based design which is executed on FPGA(Zynq7000 family) with the help of Xilinx Vivado IDE tool. Direct form poly-phase filter structure is aabsolutely preferable for wireless communications i.e, RRC interpolator.

Keywords* — *Reconfigurable filter, pulse-shaping finite impulse response (FIR) interpolator, constant multiplier (CM), wireless communication standards

I. INTRODUCTION

In this high-tech domain, there is growing request for re-usable ideas outstanding to the enlightened. Certainly, we are viewing this need for reconfigurable designs is based on cognitive (software defined), resourceful algorithms [1]. As indicated in [2], the conception of software defined radio (SDR) is to make a gemstone chip which is skilful to support multi-standard wireless communication. Hence, this transitory motivates one to design this filter which can be competently reconfigured with respect to control parameters such as roll-off factors and interpolation factor of respective filter lengths obtained from different wireless communication standard's specifications.

Since quickness in web browsing, several great data transfer rates, and fast video streaming have become key rudiments of technology fans. However, in a mixed environment, to provide guaranteed stability and multi standard wireless communication the FIR multirate filter plays a dynamic role. To control ISI caused by the multi-path signal reflections in latest devices like smart phones, the pulse-shaping FIR filters having gaining more demand. Consequently, in wireless communication systems mostly used matched filter is RRC filter is one of the commonly found pulse-shaping filters, because of its capability to increase the bit rate, bandwidth limitation and bit error rate (BER) [3].

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II. PLANNED SOLUTIONS OF THE RECONFIGURABLE FILTER

Filer Specifications are shown in table I

TABLE I

FILTER SPECIFICATIONS

Roll-off factor(α) = 0.22/0.35	WCDMA	UMTS			DVB			LTE	
Interpolation Factor (L)	4	4	6	16	6	4	3	10	13
Symbol Rate (MSPS)	1.25	3.84			27.5	42.25	55	24	26.1
Sampling Frequency (MHz)	5	15.36	30.72	61.44	165	165	165	240	339.3
Filter Lengths or Taps (N)	25	25	49	97	37	25	19	61	79

The proposed solution with respect to each design consideration

The solutions for the above described challenges are mentioned below.

1) multiplexers are used to design the two coding pass blocks to select the filter constants with respective control parameter as selection line. Thus, these multiplexer-based hardware architectures will improve the proposed filter design by reducing the need of the multiplier by 86.8%. Moreover, the proposed architecture also states that by considering more number of filter sin the design one can reduce themultiplication per input sample(MPIS) and addition per input sample (APIS).The general equation of the proposed reconfigurable channel filter is

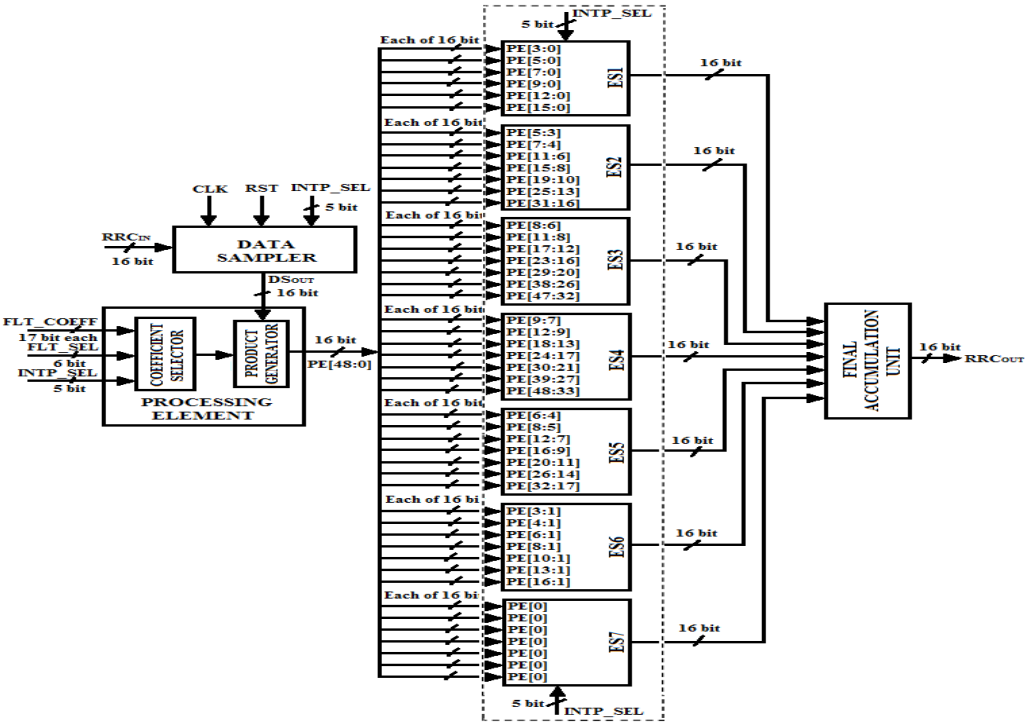

Fig. 1. Block diagram of new reconfigurable filter

$$Y= x+2^{-1} x+ 2^{-2} x+ 2^{-3} x+\cdots+2^{-14} x+ 2^{-15} x \ldots\ldots (3)$$

As the proposed architecture considers 2-bit BCS i.e.,

$Z_2= x+2^{-1} x$ .....(4)

By substituting (4) in (3), we obtain

$Y= Z_2+2^{-2}Z_2 +2^{-4}Z_{2+}...+2^{-10}Z_2+ 2^{-12}Z_2+ 2^{-14}Z_2$ .....(5)

Design of new Reconfigurable Filter

When a N-tap filter is designed by using N MAC units which leads to an increase in hardware utilization and decrease in operating frequency. The Block diagramcontains4 main blocks.

Those are:

Data sampler (DS).

Processing element (PE).

Element selector (ES).

Last accumulation unit (LA).

A. Data Sampler (DS) Block

The Fig. 2 represents the DS block diagram, samples the input data for any consider clock sources mentioned in fig2.

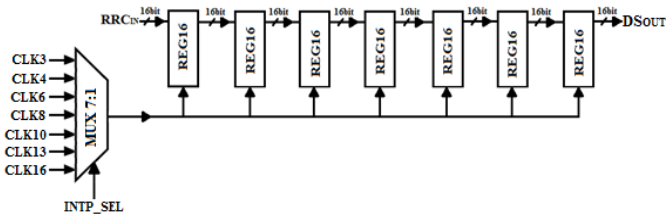

Fig. 2. Block diagram of DS

B. Processing Element (PE) Block

Selects the filter coefficients then multiply it with the data sample using PE block. To catch the pulse-shaped and interpolated product element PE block is used. So, depending upon the optimization techniques, we can classify processing element into two sub-sections.

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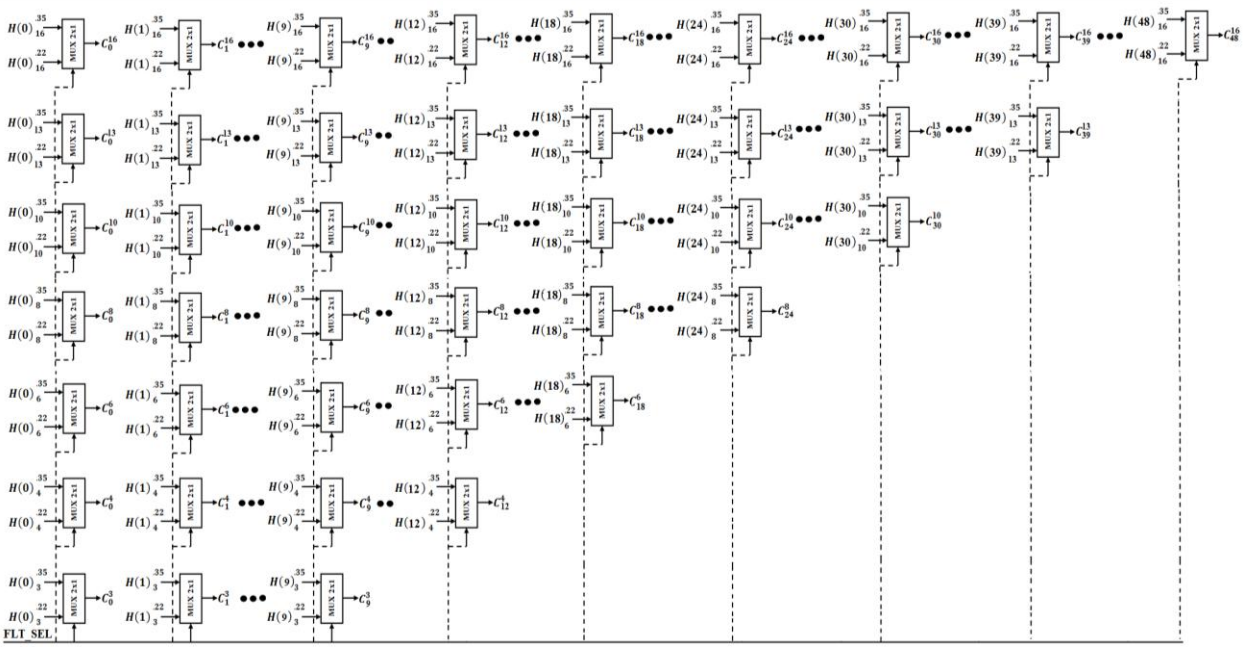


Fig.3. Block diagram of PCP

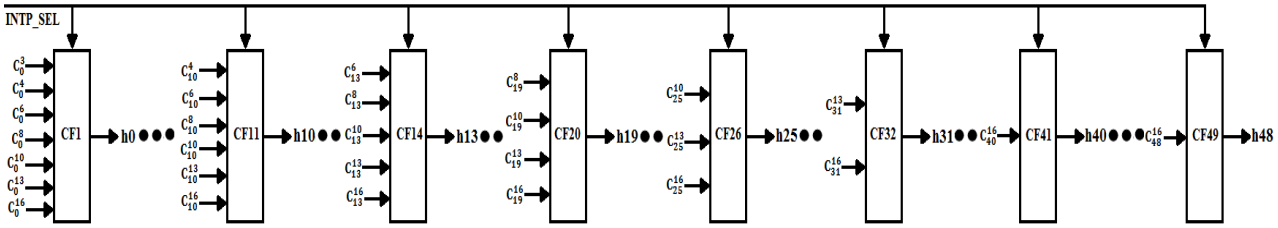


Fig.4. NCP block diagram

i. Principal Coding Pass (PCP)

PCP block architecture is shown in Fig. 3.Shows In total, the initial required number of coefficients is 734 but we consider only 187coefficients because of the symmetric property of the FIR filter. Along with this, the multiplexing technique used in the design helps to decrease the requirement of the multiplier by 74.5%. Therefore, the reduction in switching activity of the coefficients helps to reduce power consumption of the proposed design.

ii. Next Coding Pass (NCP)

NCP block architecture is shown in Fig. 4. The seven sets of multiplexed coefficients obtained from PCP block of 10, 13, 19, 25, 31, 40 and 49 in number are inputs to the NCP block to obtain final set of filter coefficients as control parameter. This way lessens the filter coefficients from 187-49 constants. So, the CS block reduces the requirement of multiplier to 93.3% .

iii. 2-Bit BCSE Algorithm Based Constant Multiplier

The proposed CM consists of two layers where the BCSE algorithm is applied in the first multiplexer layer to select partial products (PPs) and the second addition layer is used to summate the selected PPs. The data flow

diagram of the CM is shown in Fig. 5. According to the flow, the CM has different sub-modules and each sub-module will have their respective functions to provide proficient hardware utilization. In simple words, this multiplication unit can be said as product generator of the proposed design.

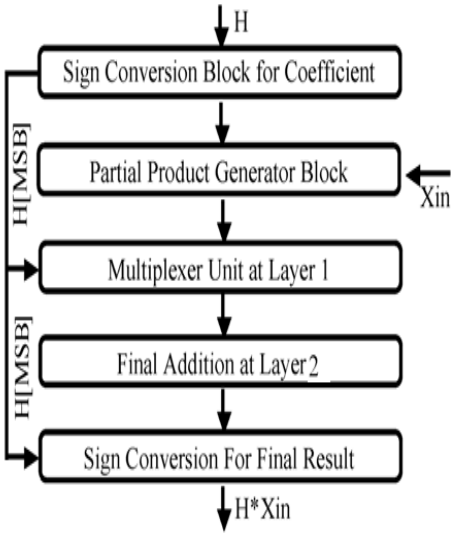


Fig.5. Dataflow diagram of 2-bit BCSE algorithm based CM

iv. Sign Alteration circuit

The sign alteration circuit is designed to get the signed decimal representation of input data and filter coefficients. The Fig. 6 represents the hardware design of the sign alteration block.

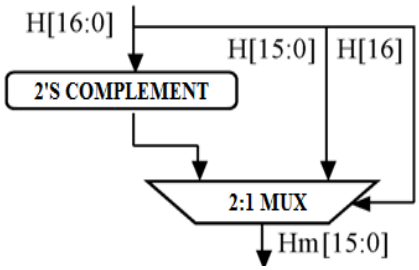


Fig.6. The block diagram of the sign alteration circuit

v. Partial Product Generator (PPG)

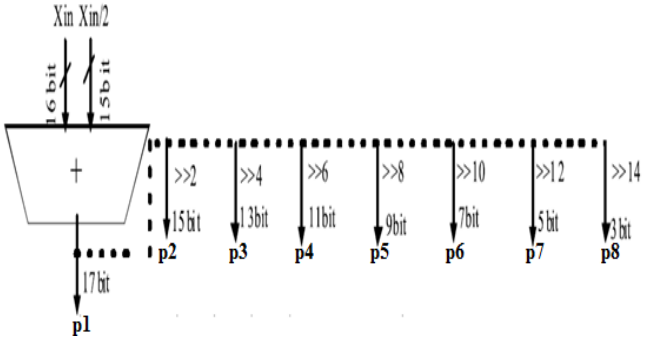


Fig.7. PPG Block architecture

The PPG architecture shown in Fig. 7 is based on shift and add technique. The generated PPs are convoluted and summated in the CM architecture to generate final multiplication output. The number of PPs generation possibility is defined according to the choice of BCS length as well as the complexity level of the multiplier can be expressed with reference to adder steps.

vi Summation Unit

The architecture present in Fig.8 itself shows the second layer of the CM, i.e., used to add the all outputs got from layer-1. The summing unit arrangements multiplication adder tree (MAT) using six adders.

vii Last Accumulation (LA) Unit

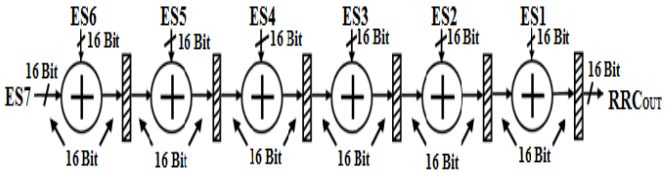


Fig. 8. Hardware architecture of LA unit

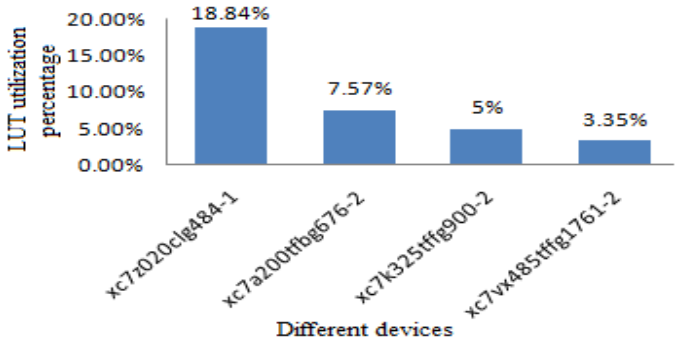
III. RESULTS AND ITS INTERPRETATION

The projected filter is realized on FPGAzynq7000 family developed kit of device xc7z020clg484-1 using Xilinx Vivado 2015.2, with Verilog HDL. The judgments of the proposed design are done seeing the input word length of 16-bit and coefficient word length of 17-bit where the MSB is used as signed bit for decimal data representation. The tabular form of device utilization summary is presented in Table II. This tabular form predicts the number of filp-flops (FF), LUTs, gated buffers (BUFG) and IOB. It also shows the percentage utilization of each resource.

TABLE II

DEVICE UTILIZATION SUMMARY OF PROPOSED DESIGN

Resource	Utilization	Available	Utilization %
FF	464	106400	0.44
LUT	10023	53200	18.84
I/O	16	200	8.00
BUFG	1	32	3.12



IV. CONCLUSION

This paper describes the design challenges that can be faced by the designer while implementing the reconfigurable filter architecture, which is a significant component in communication systems like SDR. Beside to this, the paper also provide sproposed keys to the discussed issues in the form of RRC FIR interpolation filter architecture. In count, the design have pipeline technique, which helps in sinking critical path of the design. Then, well-suited VLSI architecture of reconfigurable FIR filter is presented for 3G/4G wireless communications.

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