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REALIZATION OF TUNABLE UNIVERSAL FILTER

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ABSTRACT

This paper provides a voltage mode (VM) multi input single output (MISO) universal filter with the help of voltage differencing inverting buffer amplifier (VDIBA). All the filter functions i.e., Low pass, band pass, band reject, high pass, and all pass filter functions can be realized without modifying the circuit configuration. The pole frequency can be independently tunable by its transconductance parameter. The filter circuit requires no component matching constraint and enjoys low sensitivity figures. Functionality of proposed filter is verified by presenting the simulation results using Tanner EDA tool and 180nm technology parameters.

Terms- Tunability, Universal Filter, VDIBA.

I. INTRODUCTION

Analog active filters are popular and standard topic for circuit design. It is widely used for their important requirements for application in electrical and electronic system. Filters have wide applications such as in communications, measurement, instrumentation, and control systems. Literature shows that special attention has been given over the realization of multifunction filters or universal filter. Among various topologies of universal filter multiple-input single-output (MISO) analog filter is an important category in which various filter functions are realized at single output port by appropriate selection of input variables.

Presently numerous analog building blocks such as VDTA, VDIBA, VDBA, OTA etc. are popular in realization of various signal processing and generation circuits. Voltage differencing inverting buffer amplifier (VDIBA) is one of simpler and high performance analog building block. Due to its low transistor count and tunability feature it is gaining wide popularity among analog designer. Some of the drawbacks in the reported filter such as: independently tuned filter parameter, cascadability input/output port impedance etc.

The purpose of this paper is to overcome the aforementioned drawbacks The proposed MISO VM filter consists of two VDIBA and two capacitors only. The proposed filter circuit offers following advantages features (1) realization of all the filter functions from same configuration (2) independent tuning of pole frequency (ω_0) and bandwidth (BW) (3) no need of any matching condition (as required in most of the earlier reported MISO-type configurations), and (4) low sensitivity figure. The workability of proposed filter has been established by TANNER EDA simulations using 180nm technology parameters.

II. VDIBA

The VDIBA is recently introduced new active element. The block contains four ports and is associated with the feature of electronic tuning. Symbolic model and behavioral structure of VDIBA is depicted in Fig.1 and Fig.2

respectively. In this configuration, v_+ and v_- terminals are high impedance input ports, z is high impedance current output port and w_- is low impedance output voltage port. A VDIBA basically consist of an operational transconductance amplifier (OTA) in its input stage (Fig.3). It processes the input voltage differentially and delivers the current at z port of VDIBA. The OTA is followed by a unity gain inverting voltage buffer (IVB) amplifier, which provides voltage inversion between port z and w.

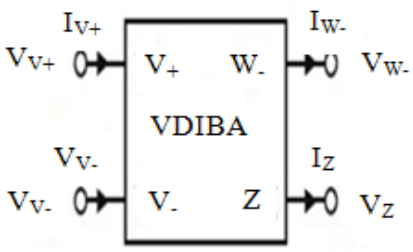

Fig. 1: Symbol of VDIBA

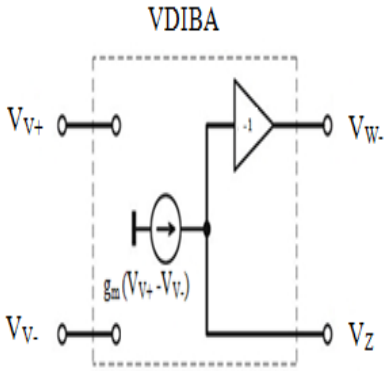

Fig. 2: Behavioral model of VDIBA

Port relation of VDIBA is described by the following matrix:

$$\begin{bmatrix} I_{v+} \\ I_{v-} \\ I_z \\ V_{w-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ g_m & -g_m & 0 & 0 \\ 0 & 0 & -\beta & 0 \end{bmatrix} \begin{bmatrix} V_{v+} \\ V_{v-} \\ V_z \\ I_{w-} \end{bmatrix}$$

Where, β and g_m describe the voltage gain and transconductance of VDIBA respectively. The value of β ideally is unity. It can be seen that port z current is controlled by transconductance parameter g_m which in turn is controlled by the bias current (I_B).

The CMOS implementation of the VDIBA is showing in Fig.3.The circuit consists an active loaded differential pair (transistors M_1 and M_4) followed by a unity gain inverting voltage buffer (IVB) (matched transistors M_5 and M_6).

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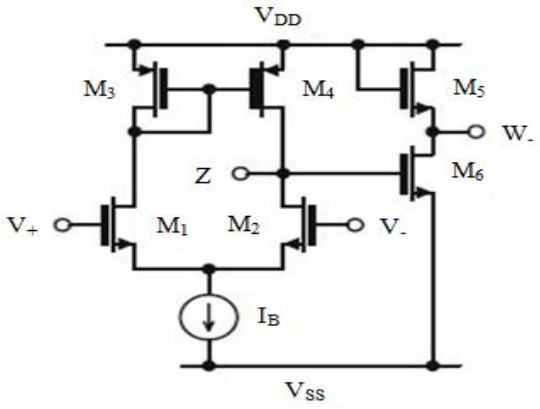

Fig. 3: CMOS structure of VDIBA

III. PROPOSED UNIVERSAL FILTER

Fig. 4 shows the proposed multi input signal output (MISO) voltage mode (VM) universal filter. It comprises two capacitors and two VDIBA. It is three inputs and one output device. Proposed filter configuration realizes all the responses in inverting and non- inverting modes. The biquad filters have property of low output impedance which is an essential factor for cascadability for VM circuit

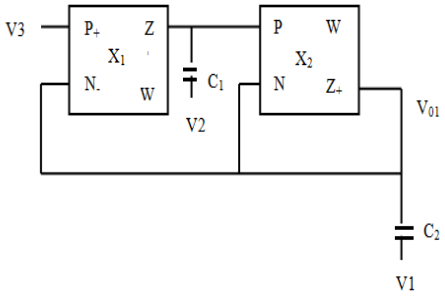

Fig. 4: Proposed VM biquad filter

The output voltage of the proposed filter can be given as:

$$V_o = \frac{s^2 V_1 + s\frac{g_m}{C} V \quad (1) \quad \frac{g_{m1} g_{m2} V_3}{C_1 C_2}}{s^2 + s\frac{g_{m2}}{C_2} + \frac{g_{m1} g_{m2}}{C_1 C_2}}$$

It can be viewed from (1) that all the filter function can be realized by the design filter from the same topology without the requirement of any component matching condition.

From (1), the natural frequency is given as

$$w_o = \sqrt{\frac{g_{m1} g_{m2}}{}} \quad (2a)$$

Subsequently, the quality factor is given as

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$$Q = \sqrt{\frac{}{g_{m_2} C_1}} \quad (2b)$$

Bandwidth is given as

$$BW = \frac{}{C_2} \quad (2c)$$

It is evident from (2a) and (2b) that the natural frequency and quality factor can be electronically tuned via g_m.

Table I shows realization condition for various input combinations for all filter functions

Table I: Input set for different filter functions

S.NO.	INPUT	FILTER FUNCTION
1	$V_1=V_2=0, V_3=V_{in}$	LP
2	$V_2=V_3=0, V_1=V_{in}$	HP
3	$V_1=V_3=0, V_2=V_{in}$	BP
4	$V_2=0, V_1=V_3=V_{in}$	BR
5	$V_1=(-V_2)=V_3=V_{in}$	AP

It can be seen from (1) that BW and ω_0 of proposed filter can be tuned independently by first setting the BW by gm_2 and then varying ω_0 by g_{m1}. The value of Q can be set by capacitance ratio C_2/C_1. The analysis of sensitivity with respect to active and passive element for the proposed filter is less than 1.

Sensitivity of the above equation is given below:

$$S^{\omega 0}_{g1,g;} \quad (3a) \quad {}^{\omega 0}_{1,C2} = \frac{1}{2}$$

$$S^{Q}_{g1,C;} \quad (3b) \quad {}_{2,C1} = \frac{1}{2}$$

IV. COMPARISON

The proposed filter configuration is compared with previously designed filters in Table II on the basis of following important features such as (1)Independently tuned filter parameter (2) Appropriate input port impedance (high-for voltage, Low for current Grounded/floating) (3) Appropriate output port impedance-(Low-for voltage, High for current) (4) Component Matching constraints (5) No of resistors (Grounded/ floating) (6) No of capacitors (Grounded/ floating) (7) No of filter functions –Low pass, High pass, Band pass, Band stop, All pass (8) Mode of operation (CM/VM) (9) No of active elements with name.

It can be viewed that the designed filter provides better features, as compared to the other filters listed in Table II, which lacks one or more important features.

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V. SIMULATION RESULTS

To validate the proposed configuration, simulation results are presented in this section using Tanner EDA tool. Supply voltage is set to 0.9V. The aspect ratios of the OTA transistors (M_1-M_4) and the IVB (M_5 and M_6) has been taken as W/L (M_1-M_4)=18µm/1.08µm and W/L(M_5,M_6)=54µm/0.18µm. The transconductance (g_{m1}, g_{m2}) of VDIBA has set to 656.01µA/V. The bias currents has been selected as I_B =100 µA. The value of passive components C_1 and C_2 is taken as 10pf and 5pf respectively. The transconductance are controlled by bias currents of VDIBA. Fig. 5 and 6 depict the simulated filter responses of LP, BP, HP, BR and AP. Selected component values results in Q = 0.707, f_0= 3.41MHz and 3.53MHz, and BW= 15MHz for equal bias current i.e. for g_{m1} and g_{m2}. These result, thus confirms the validity of designed filter.

At I_b=100μA the frequency is 3.41MHz.

Features/ References	1	2	3	4	5	6	7	8	9
1	N	N	N	N	0/1	0/2	5	VM	1(VDIBA)
2	Y	Y	N	Y	0/1	0/2	5	VM	1 (VDIBA)
3	N	N	N	N	0/1	0/2	5	VM	1(VDIBA)
4	Y	Y	N	Y	0/2	2/0	5	VM	2(VDTA)
5	N	N	N	N	0/0	2/0	3	VM	1(VDTA)
6	Y	N	N	Y	1/0	2/0	5	VM	1(VDTA)
7	N	Y	N	Y	0/0	2/0	5	CM	1(VDTA)
Proposed	Y	Y	Y	N	0/0	0/2	5	VM	2(VDIBA)

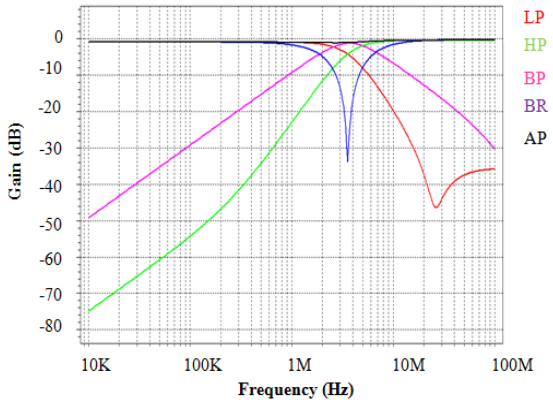

Fig.5: Frequency response of proposed universal filter

At I_b =150μA the frequency is 3.53MHz.

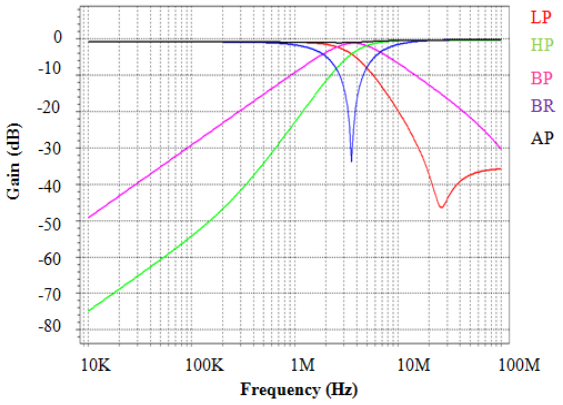

Fig.6: Frequency response of proposed universal filter

VI. CONCLUSION

The proposed circuit uses two capacitors and two VDIBAs only. The circuit has the capability to realize all the functions of the filter without modifying circuit topology. The circuit has independent electronic tuning between pole frequency and Bandwidth. Moreover, the configuration requires no component matching constraints and has low active and low passive sensitivities. The performance of the designed circuit is verified by tanner simulations using 180nm technology.

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