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128 BIT MODIFIED SQUARE ROOT CARRY SELECT ADDER

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ABSTRACT

Toperform fast arithmetic functions in data processing processors carry select adders are used. Carry select adder(CSLA)is used to increase the speed of a parallel adder that expands area in favour of speed .CSLA is used in many computational systems to diminish the problem of carry propagation delay by seperately generating multiple carriers and then select a carry to generate the sum. The problem coming in CSLA is not area efficient because it uses multiple pairs of Ripple carry adders (RCA) to generate the partial sum and carry which are selected by the multiplexer. Square Root CSLA is constructed by equating the delay through two carry chains and the block multiplexer signal from previous stage. This is an extension of linear CSLA which improves the delay time greatly. By using SQRT CSLA, the time waiting for carry bit is used to calculate an extra input bit in each stage, hence the time can be improved.

Keywords: Array signal processing, Broadcast channels, co channel interference, diversity methods, feedback communication.

I. INTRODUCTION

In digital circuits,by the time required to propagate a carry through the adder the speed of addition is limited. The circuit architecture is simple and area-efficient. The sum for each bit position in an elementary adder is generated consequently only after the previous bit position has been summed and a carry propagated into the next position. The serious speed limitation in any adder is in the production of carries and many authors considered the addition problem. To solve the carry propagation delay CSLA is progressed which drastically reduces the area and delay to a great extent.However, the Regular CSLA is not area and speed efficient because it uses the numerous pairs of Ripple Carry Adders (RCA) to generate partial sum and carry by considering carry input. The last sum and carry are selected by the multiplexers (mux). Due to the use of two seperate RCA the area will increase which leads to an increase in delay. To overcome the above problem, the basic idea of the proposed work is to use n-bit binary to excess-1 code converters (BEC) to enhance the speed of addition. This logic can be exchanged in RCA for Cin=1 to further improves the speed and thus reduces the delay. Using Binary to Excess -1 Converter (BEC) instead of RCA in the regular CSLA will achieve lower area, delay which

speeds up the addition operation. The main advantage of this BEC logic comes from the lesser number of logic gates than the FullAdder (FA) structure because the number of gates used will be decreased.

II. RELATED WORK

(A) FULL ADDER

Full adder is for adding three inputs and to produce a SUM and a CARRY outputs. Full adder is mainly needed to add large number of bits. E.g. consider happens to other bits until the MSB is reached. So full adder is the important component in binary additions. A half-adder can only be used for LSB additions. Figure shows the truth table, K-maps and So, to add the next bits, we need to add three bits with carry from former addition. Same things recorded and the carry is forwarded to the next bits. Boolean expressions for the two output variables, SUM and CARRY outputs of full adder.

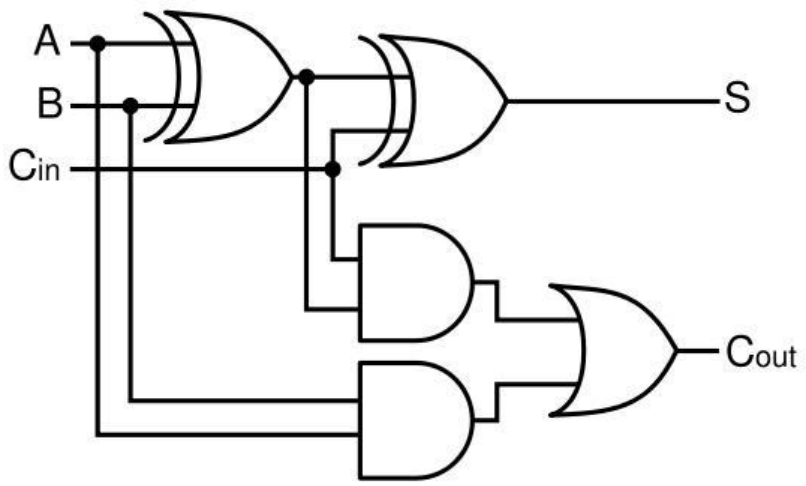

Fig.(A) logic diagram of full adder

(B) RIPPLE CARRY ADDER

Half Adders are used in adding two one bit binary numbers. It is also possible to create a logical circuit using multiple full adders to add N-bit binary numbers.Each full adder inputs a **Cin**, which is the **Cout** of the previous adder. This kind of adder is a **Ripple Carry Adder**, since each carry bit"ripples" to the next full adder. The layout of ripple carry adder is simple, which allows for fast design time; however, the ripple carry adder is relatively slow, because each full adder must wait for the next carry bit to get calculated from the previous full adder. The gate delay can easily be calculated by inspection of the full adder circuit. Each full adder requires three levels of logic.

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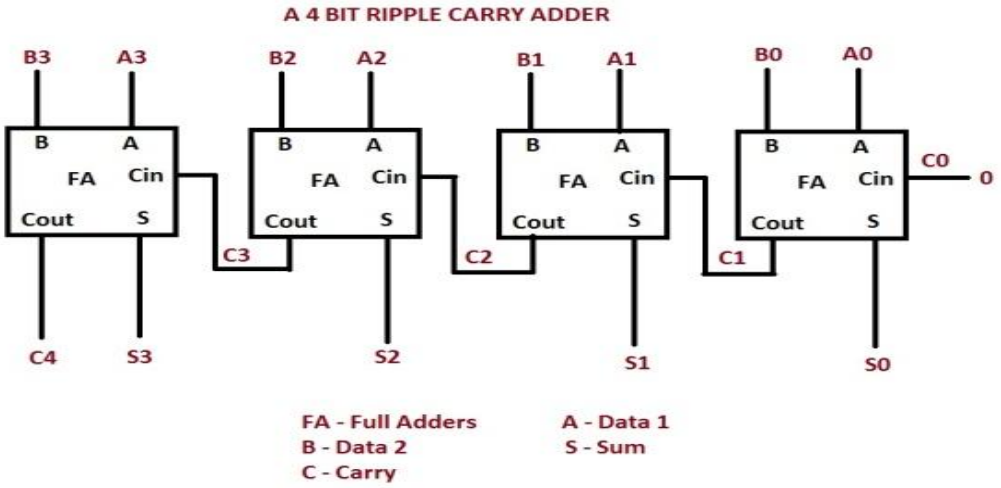

Fig.(B) Ripple carry adder

(C) BINARY TO EXCESS 1 CODE CONVERTER

The basic idea of this modified work is to use binary to excess 1 converter instead of ripple carry adder(RCA) with Cin=1 in the regular CSLA to achieve a low area and power consumption with only a slight increase in the delay. The main asset of this BEC logic comes from the lesser number of logic gates than the n-bit full adder. The importance of the BEC logic stems from the large silicon area reduction when the CSLA with large number of bits are designed. The Boolean expressions of the 4-bit BEC is listed as (note the functional symbols NOT, & AND, XOR) X0 = ~B0 X1 = B0 ^ B1 X2 = B2 ^ (B0 & B1) X3 = B3 ^ (B0 & B1 & B2).

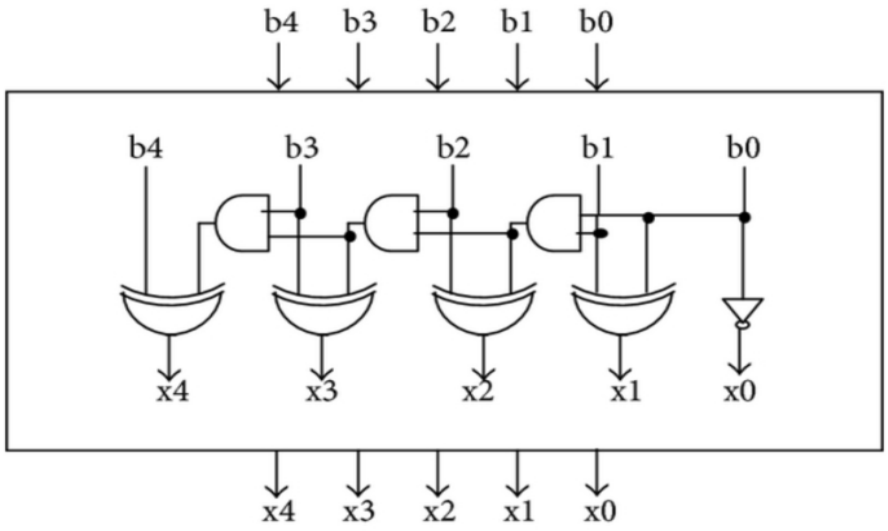

Fig.(C) Binary to excess 1 converter

(D) MULTIPLEXER

In the field of electronics , a multiplexer (mux) is a device that selects one of several analog or digital input signals and forwards the selected input into a single line. A multiplexer of 2^n inputs has n select lines, which are

used to select which input line to send to the output.All the multiplexers are mainly used to increase the quantity of data that can be sent over the network within a certain amount of time and bandwidth. A multiplexer is also called a **data selector**.

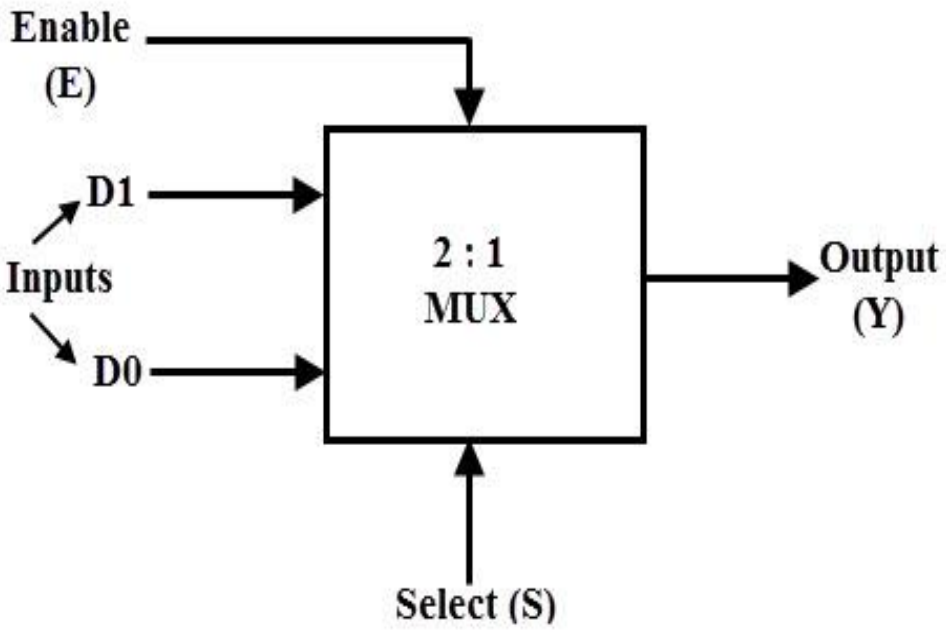

Fig.(D) Block diagram of 2:1 mux

III. PROPOSED SYSTEM

(A)REGULAR SQRT CARRY SELECT ADDER

The fundamental square-root Carry Select adder has a dual ripple carry adder with 2:1 multiplexer, the main disadvantage of regular CSLA is the large area due to the numerous pairs of ripple carry adder. These 16-bits are divided into five groups with different bit sizes of ripple carry adders . From the regular SQRT CSLA, there is scope for making lesser delay and area utilization. The carry out is calculated from the last stage, in this the selection is done by using a multiplexer.

(B)MODIFIED SQRT CARRY SELECT ADDER

The main concept of this work is to use BEC instead of the RCA with Cin=1 in order to reduce the delay and area utilization of the regular SQRT CSLA. To replace the n-bit RCA, a n+1 bit BEC is required. The structure of a 4-bit BEC illustrates how the basic function of the CSLA is obtained by using the 4-bit BEC together with the mux. In this structure one input of the 8:4 mux gets as it input (B3, B2, B1, and B0) and another input of the mux is the BEC output. This produces the two feasible partial outputs in parallel according to the control signal

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Cin. The importance of the BEC logic stems from the large silicon area reduction when the CSLA with large number of bits are designed. The structure is again segregated into five groups with different sizes of

separate groups of both regular and modified SQRT input to the multiplexer goes from the RCA with CSLA, it is clear that the BEC structure lowers the delay. But the disadvantage of BEC method is that the area is increasing than the regular SQRT CSLA.Ripple carry adder and BEC.. The parallel Ripple carry adder with Cin=1 is replaced with BEC. One Cin=0 and other input from BEC. Comparing the

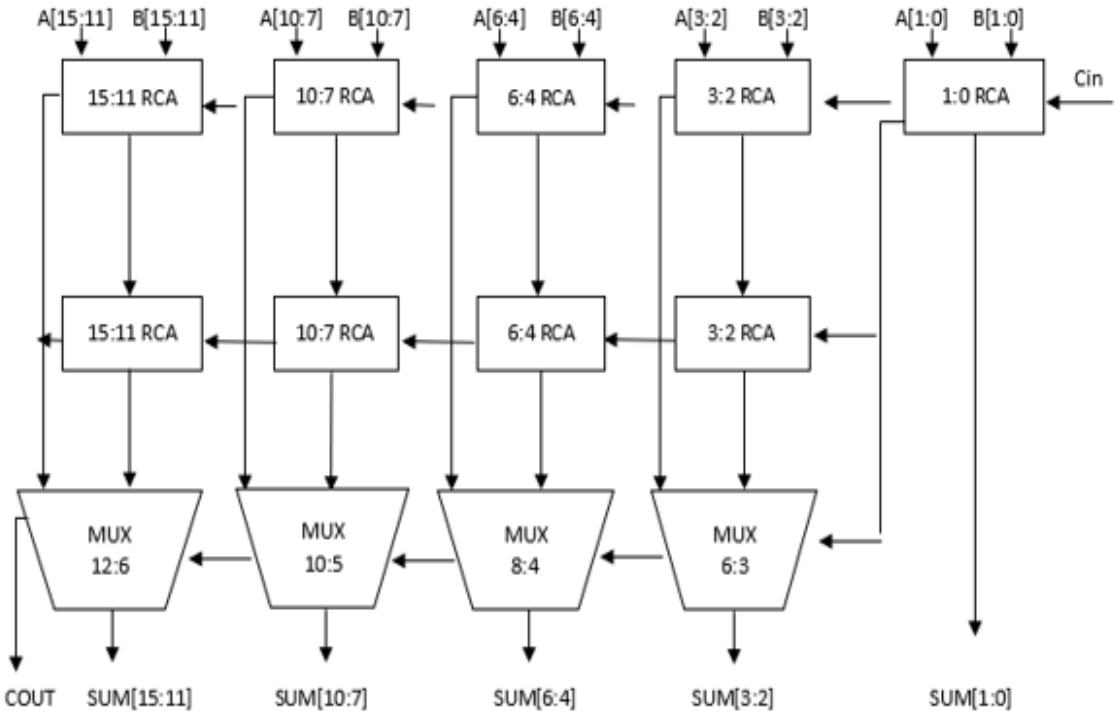

Fig.(A) 16 bit regular sqrt carry select adder

IV. ARCHITECTURE OF 128 BIT MODIFIED SQRT CARRY SELECT ADDER

The modified 64-bit SQRT CSLA is generated using two 32-bit modified SQRT CSLA. The 128-bit SQRT CSLA is constructed using the two 64-bit SQRT CSLA with the carry input cin=1 and the power is reduced very much and the area occupied is also very less. The area of the modified SQRT CSLA is very less when contrasted to the regular SQRT CSLA. From the simulation results the area of the modified 128-bit SQRT CSLA is greatly reduced when compared to the area occupied by the regular 128-bit SQRT CSLA.

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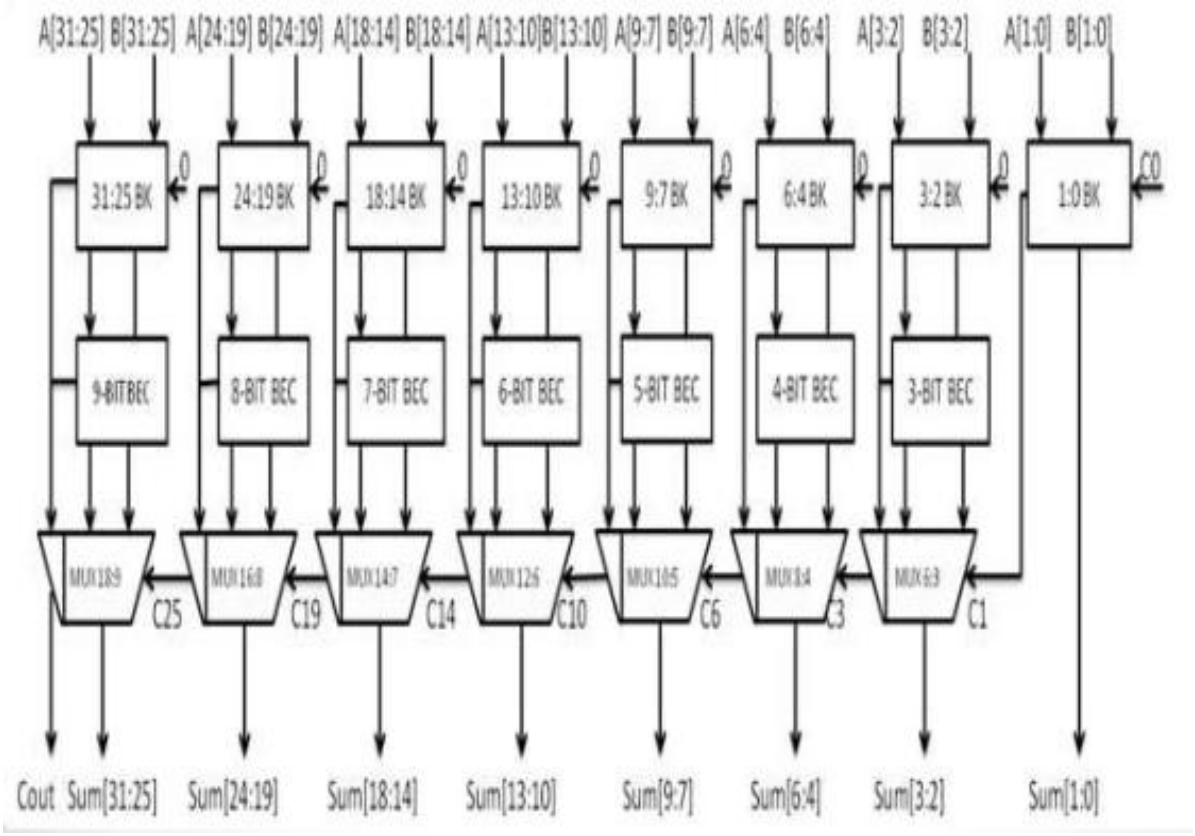

Fig.IV. 16 bit modified sqrt carry select adder.

V. COMPARISON OF REGULAR AND MODIFIED 128 BIT SQRT CSLA

Comparison of Regular and modified 128-bit CSLA. The delay overhead for the 8, 16, and 32-bit is 15%, 9.7%, and 5.43% respectively, whereas for the 64-b it reduces to only 5.75%. The power–delay product of the proposed 8-b is higher than that of the regular CSLA by 4.2% and the area -delay product is lower by 2.8%. However, the power-delay product of the proposed 16-b CSLA reduces by 1.66% and for the 32-b and 64-b by as much as 8.28%, and 11.28% respectively. Similarly the area-delay product of the proposed design for 16-bit, 32-bit, 64-bit and 128-bit is also reduced by 6.7%, 11%, and 14.4% respectively.

ADDERS		DELAY(ns)	AREA(μm^2)
32-BIT	REGULAR	20.05	91
	MODIFIED	14.24	87
64-BIT	REGULAR	33.85	185
	MODIFIED	28.25	180
128-BIT	REGULAR	40.35	440
	MODIFIED	32.51	435

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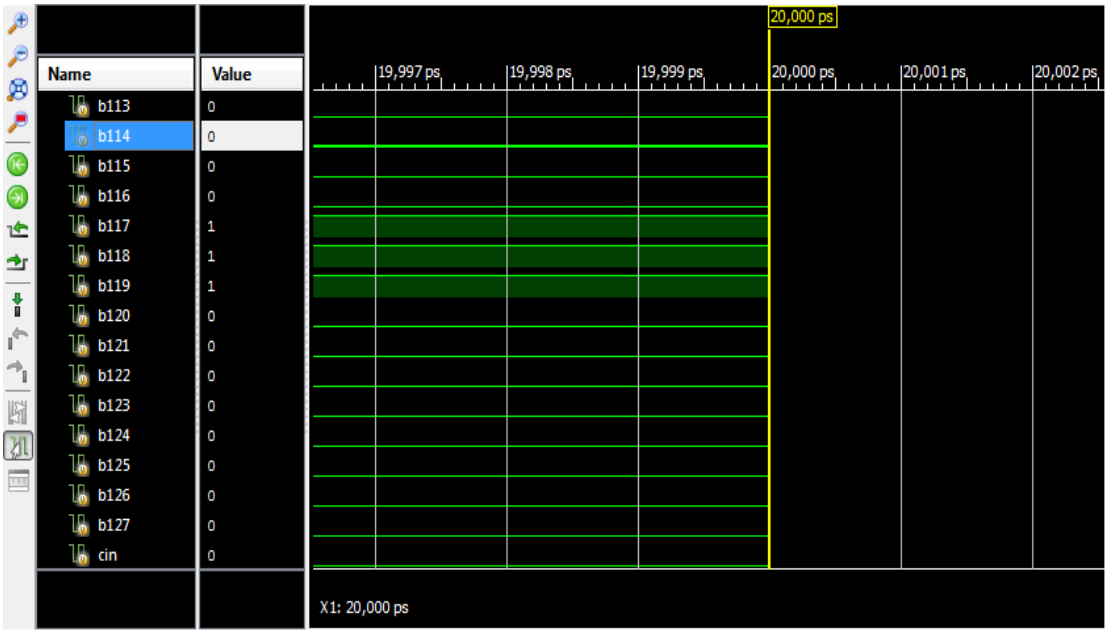
VI. RESULT ANALYSIS AND FUTURE SCOPE

The implemented design in this work has been simulated using Verilog-HDL (Modelsim). The simulated files are imported into the synthesized tool and corresponding values of delay and area are noted. The synthesized reports contain area and delay values for modified SQRT root CSLA.The 128 bit modified square root carry select adder yields better architecture and lowers the delay and area better than the linear carry select adder and regular square root carry select adder. The SQRT CSLA using BEC's can be used in many processing processors in order to achieve quick performance. The Area and Power can be reduced. We also conclude that this addition technique can be implemented for large higher values of bits.



The adders 128 BIT are designed and simulated using Modelsim. After simulation the different size codes are synthesized using Xilinx ISE 10.

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