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A POWER EFFICIENT AND ENHANCED VLSI ARCHITECTURE FOR VEDIC MULTIPLIER

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ABSTRACT

In most of digital signal processing systems and in general processors a high speed processor is used as it is one of the key hardware block. This paper presents a high speed Vedic multiplier architecture which is quite different from the Conventional method of multiplication like shift and add. The developed multiplier architecture is based on Vertical and Crosswise structure of Ancient Indian Vedic Mathematics this is the most significant aspect of the proposed method. All partial products and their sum can be generated in one step. This also gives rise to modular design in which smaller block can be used to design the bigger one. Through this the design complexity gets reduced for inputs of larger number of bits and modularity gets increased. The proposed Vedic multiplier is coded in VHDL (Very High Speed Integrated Circuits Hardware Description Language), synthesized and simulated using EDA (Electronic Design Automation) tool – XilinxISE14.5. The results are then compared with Conventional multipliers to show the significant improvement in its efficiency in terms of path delay (speed). The Vedic Multiplication technique is very much suitable for high speed processor which requires high speed multipliers.

Keywords: Architecture, Ripple Carry (RC) Adder, Multiplication, Vedic Mathematics, Vedic Multiplier (VM), Urdhava Tiryakbhyam Sutra

I.INTRODUCTION

In Microprocessors, DSP and Communication applications multipliers have been extensively used. For higher order multiplications, to perform the partial product addition a huge number of adders are being used. The need for high speed multiplier is increasing as the need of high speed processors are increasing. The development of fast multiplier circuit has been a subject of interest over decadesand one of the key arithmetic operations in such applications is multiplication. The essential requirements for many applications are reducing the time delay and power consumption **.**In the past multiplication was implemented generally with a sequence of addition, subtraction and shift operations. Array multiplication algorithm and Booth multiplication algorithm are the two most common multiplication algorithms followed in the digital hardware .Digital multipliers, due to its importance in DSP, it has always been an active area of research .The name given to the ancient system of mathematics is the Vedic mathematics, which was rediscovered from theancient Indian scriptures between 1911 and 1918 by Jagadguru Swami Sri BharatiKrisnaTirthaji (1884-1960), a scholar of Sanskrit, mathematics, history and philosophy.

The paper is organized as follows. Section II describes the basic methodology of Vedic multiplication technique. Section III describes the proposed multiplier architecture based on Vedic multiplication and the generalized algorithm for NxN bit Vedic multiplier. The design and implementation of Vedic multiplier module in XilinxISE12.1 is described in section IV. Section V embraces of Result and Discussion in which device application summary and computational path delay accomplished for the proposed Vedic multiplier (after synthesis) is contended. Finally Section VI comprises of Conclusion.

II.VEDIC MULTIPLICATIONTECHNIQUE

To reduce the typical calculations in conventional mathematics to very simple one Vedic multipliers is used. It is claimed that the Vedic formulae are based on the natural principles on which the human mind works. More efficient speed implementation can be done by Vedic Mathematics through its methodology of arithmetic rules.Some effective algorithms are provided which are implemented to various branches of engineering such as computing.

A.UrdhvaTiryakbhyam Sutra

The proposed Vedic multiplier is based on the "UrdhvaTiryagbhyam" sutra (algorithm). Multiplication of two numbers in the decimal number system is done traditionally using this Sutras. In this work, same ideas are applied to the binary number system to make the proposed algorithm compatible with the digital hardware. It is a general multiplication formula that can be applicable to all cases of multiplication. It literally means "*Vertically andCrosswise*". The generation of all partial products can be done with the concurrent addition of these partial products which is based on a novel concept. This algorithm can be generalized for N x N bit number. Since the partial products and their sums are calculated in parallel, since the multiplier is independent of the clock frequency of the processor. It can be easily layout in microprocessors and designers can easily circumvent these problems to avoid catastrophic device failures, due to its regular structure. Increasing the input and output data bus widths the processing power of multiplier can easily be increased since it has a quite a regular structure. It can be easily layout in a silicon chip since it has regular structure. As the number of bits increases, gate delay and area increases very slowly as compared to other conventional multipliers, this is the advantage of multiplier based on this sutra.

B.Vedic Multiplication of two decimal numbers 252 x 846

Let us consider the multiplication of two decimal numbers 252 x 846 by Urdhva-Tiryakbhyam method to illustrate this scheme as shown in Fig. 1. From the previous step the digits on the both sides of the line are multiplied and added with the carry. One of the bits of the result and a carry is generated. The process goes on by adding the carry in next step. All the results are added to the former carry, if there are more than one line in one step. All other bits act as carry for the next step in each step and least significant bit acts as the result bit. Initially the carry is taken to be zero.

III.THE PROPOSED MULTIPLIER ARCHITECTURE

In the below sections the hardware architecture of 2X2, 4x4 and 8x8 bit Vedic multiplier module are displayed. Here, "Urdhva-Tiryagbhyam" (*Vertically and Crosswise*) sutra is used to propose such architecture for the

multiplication of two binary numbers. In Vedic multiplier, both partial product generation and additions are done concurrently. Hence, parallelprocessing is well adapted.Binary multiplications are made more attractive by this feature. The primary motivation behind this work is it reduces delay.

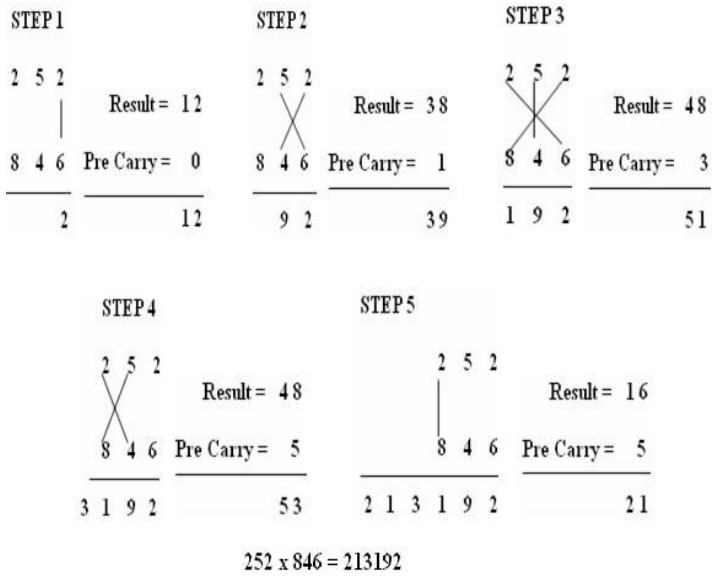

Fig. 1 Multiplication of two decimal numbers –256x846

A. Vedic Multiplier for 2x2 bit Module

The method is explained below for two, 2 bit numbers *A* and *B* where *A* = *a*1*a*0 and *B* = *b*1*b*0 as shown in Fig. 2. The least significant bits are multiplied which then gives the least significant bit of the final product (vertical). Then, the LSB of the multiplicand is multiplied with the next higher bit of the multiplier and added with, the product of LSB of multiplier and next higher bit of the multiplicand (crosswise). The sum gives second bit of the final product and the carry is added with the partial product obtained by multiplying the most significant bits to give the sum and carry. The third corresponding carry and its bit becomes sum which is the fourth bit of the final product. $S0 = a0b0$; (1)

$c1s1 = a1b0 + a0b1$; (2)

$c2s2 = c1 + a1b1$; (3)

The final result will be the c2s2s1s0. This multiplication method is applicable for all the cases.

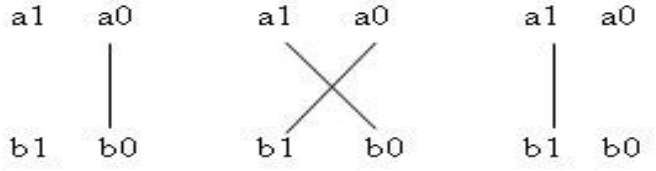

Fig. 2 The Vedic Multiplication Method for 2-bit Binary Numbers Four input AND gates & two half-adders are used to implement 2X2 Vedic multiplier module which is displayed in its block diagram in Fig. 3. The hardware architecture of 2x2 bit conventional

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Array Multiplier [2] is same as the hardware architecture of 2x2 bit Vedic multiplier. After final bit products are generated, which is very similar to Array multiplier we can state that the total delay is only 2-half adder delays. Because of this we switch over to the implementation of 4x4 bit Vedic multiplier which uses the 2x2 bit multiplier as a basic building block. The same method can be extended for input bits 4 & 8. But for higher no. of bits in iput, little modification is required

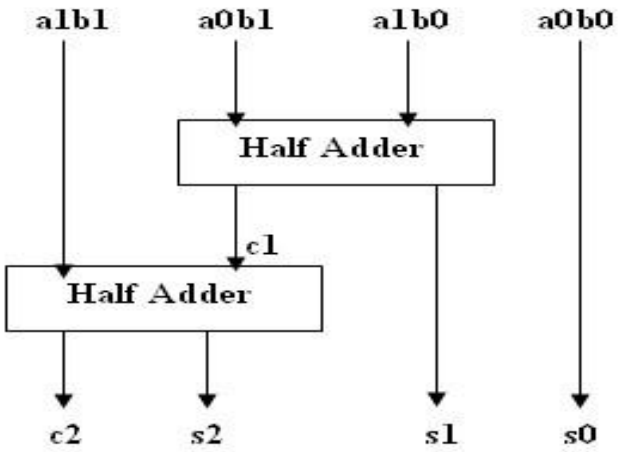

Fig. 3 Block Diagram of 2x2 bit Vedic Multiplier

B.Vedic Multiplier for 4x4 bit Module

Four 2x2 bit Vedic multiplier modules are used to implement 4x4 bit Vedic multiplier module as discussed in Fig. 3.Consider the 4x4 multiplications, say A= A_3 A_2 A_1 A_0 and B=B_3 B_2 B_1 B_0. The output line for the multiplication result is – S_7 $S_6$$S_5$$S_4$ S_3 S_2 S_1 S_0, let's divide A and B into two parts, say A_3 A_2 & A_1 A_0 for A and B_3 B_2& $B_1$$B_0$ for B. We can have the following structure for multiplication as shown in Fig. 4, by using the fundamental of Vedic multiplication, taking two bit at a time and using 2 bit multiplier block.

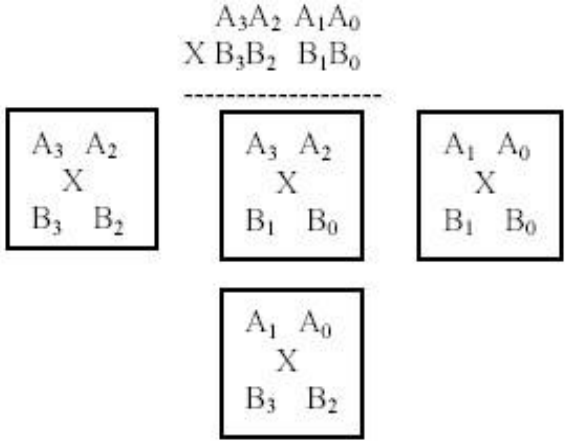

Fig. 4 Sample Presentation for 4x4 bit Vedic Multiplication

Each block as shown above is 2x2 bit Vedic multiplier. $A_1$$A_0$ and $B_1$$B_0$ are the inputs of first 2x2 bit multiplier. A_3 A_2 and B_3 $B_2$are the inputs of 2x2 bit last block multiplier. The middle one shows two 2x2 bit multiplier with inputs A_3 A_2& $B_1$$B_0$ and $A_1$$A_0$& B_3 B_2. S_7 $S_6$$S_5$$S_4$ S_3 S_2 S_1 S_0 is the final result of multiplication, which is of 8 bit. To understand the concept, the Block diagram of 4x4 bit Vedic multiplier is shown in Fig. 5.

(S_7 S_6 S_5 S_4 S_3 S_2 S_1 S_0), four 2x2 bit Vedic multiplier (Fig. 3) and three 4-bit Ripple-Carry (RC) Adders are required to get final product.

To reduce delay the proposed Vedic multiplier can be used. Based on array multiplier structures early literature speaks about Vedic multipliers. A new architecture, which is efficient in terms of speed is proposed. The arrangements of RC Adders shown in Fig. 5, helps us to reduce delay. By using four 4x4 multiplier modules we can be able to implement 8x8 Vedic multiplier modules.

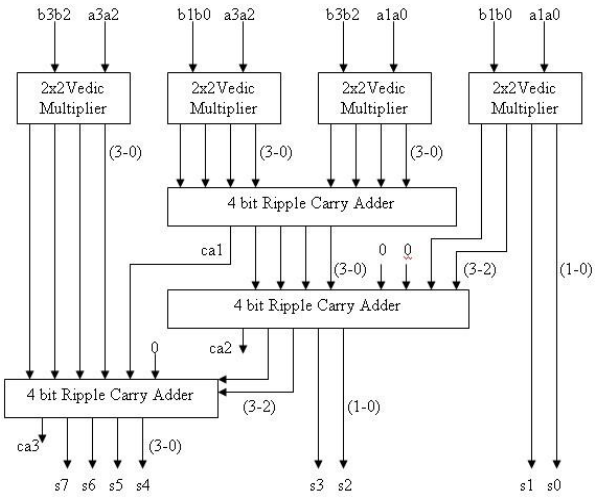

Fig. 5 Block Diagram of 4x4 bit Vedic Multiplier

C.Vedic Multiplier for 8x8 bit Module

The 8x8 bit Vedic multiplier module can be easily implemented by using four 4x4 bit Vedic multiplier modules as discussed in the previous section. Say A= A_7 A_6 A_5 A_4 A_3 A_2 A_1 A_0 and B= B_7 B_6 B5B_4 B_3 B_2 $B_1$$B_0$, let's analyze 8x8 multiplications. The multiplication result of the output line will be of 16 bits as – S_{15} S_{14} S_{13} S12 S11 S10 S9 S8 S7 S6S5S4 S3 S2 S1 S0. The 8 bit multiplicand A can be decomposed into pair of 4 bits AH-AL by dividing A and B into two parts. Similarly multiplicand B can be decomposed into BH-BL.

$$P = A \times B = (AH\text{-}AL) \times (BH\text{-}BL)$$
$$= AH \times BH + (AH \times BL + AL \times BH) + AL \times BL \quad (4)$$

Using the fundamentals of Vedic multiplication, taking four bits at a time and using 4 bit multiplier block as discussed we can perform the multiplication. To obtain the final product the outputs of 4x4 bit multipliers are added. Here total three 8 bit Ripple-Carry Adders are required as shown in figure.6.

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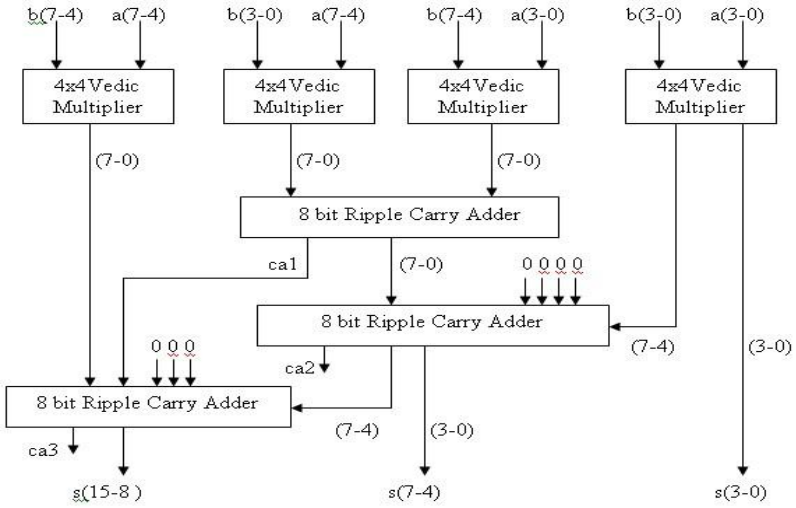

Fig. 6 Shows the block diagram of 8x8 bit Vedic Multiplier

D.Generalized Algorithm for N x N bit Vedic Multiplier

For any number of bits in input we can generalize the method as discussed in the previous sections. Let us consider the multiplication of two N-bit binary numbers (where N = 1, 2, 3…N, must be in the form of 2^N) *A* and *B* where$A = A_N.....A_3\,A_2\,A_1$ and$B= B_N….B_3\,B_2\,B_1$. The final multiplication result will be of (N + N) bits as $S = S_{(N+N)}....S_3\,S_2\,S_1$.

Step 1: The multiplicand A and multiplier B are divided into two equal parts, each consisting of [N to (N/2)+1] bits and [N/2 to 1] bits respectively, where first part indicates the MSB and other represents LSB.

Step 2: The parts of A are represented as A_M and A_L, and parts of B as B_M and B_L. A and B are represented as $A_M\,A_L$ and $B_M\,B_L$ respectively.

Step 3: For A X B, we have general format as shown in Fig.7

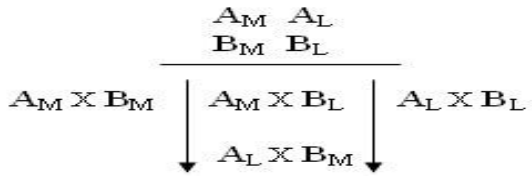

Fig. 7 General Representation for Vedic Multiplication

Step 4: By the partitioning method and applying the basic building blocks the individual multiplications product can be obtained. We can implement Vedic Multiplier for any number of bits say 16, 32, 64, and so on, as per the requirement by adopting the above generalized algorithm. It will reduce the computational speed drastically & hence improves the processors efficiency therefore, it could be possible to implement this Vedic multiplier in the ALU (Arithmetic Logic Unit).

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IV.IMPLEMENTATION IN XILINX 12.1

Let us consider a8x8 bit Vedic multiplier to be designed in VHDL. XilinxISE12.1i - Project Navigator and ISim simulator integrated in the Xilinx package. Xilinx device family Spartan3, package tq144 and speed grade -5 is used to evaluate the performance of the circuit.

The RTL schematic representation of 8x8 bit Vedic multiplier :

"vedic_multi_struct8x8" comprises of four 4x4 bit Vedic multiplier "vedic_multi_struct4x4_1" - vm1, vm2, vm3, vm4 and three 7-bit Ripple Carry Adder "rc_adder_8" - r1, r2, r3 as shown in Fig. 8 while the simulation results obtained are shown in Fig. 9 for verification. In behavioral simulation we have tested for the following input bits: -

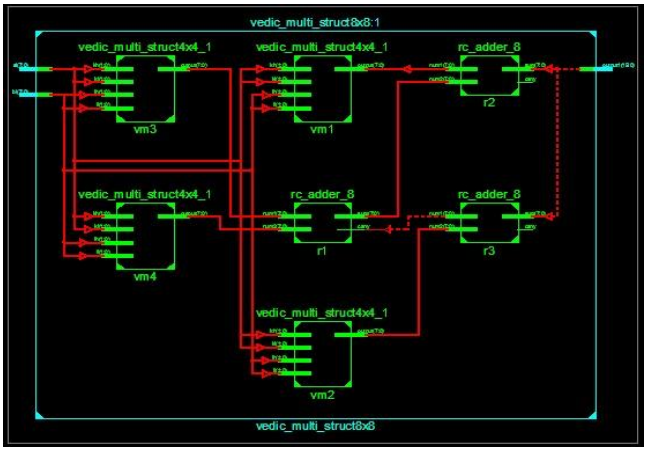

Fig. 8 RTL schematic of 8x8 bit Vedic Multiplier

a) For 8x8 bit Vedic multiplier input, the multiplier a="00000101" (decimal number system 5) and multiplicand b="00000110" (decimal number system 6) and we get 16-bit output1= "0000000000011110" (decimal number system 30).

b) Once again, we get the multiplier a=00001000" (decimal number system 8) and multiplicand b="00000110" (decimal number system 3) with 16-bit output1="0000000000011000" (decimal number system 24).

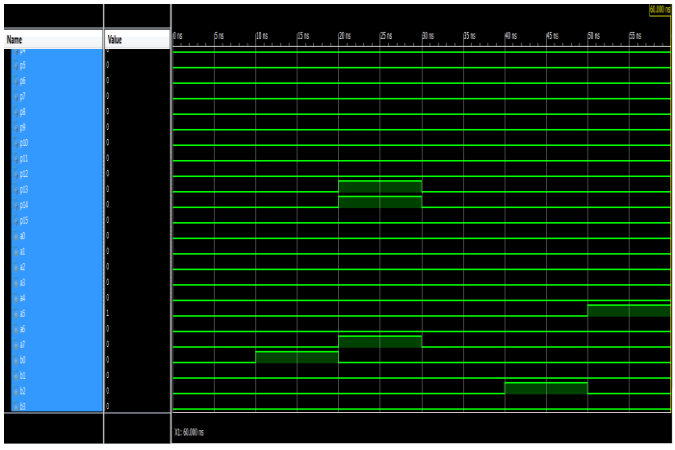

Fig. 9 Simulation Result of 8x8 bit Vedic Multiplier

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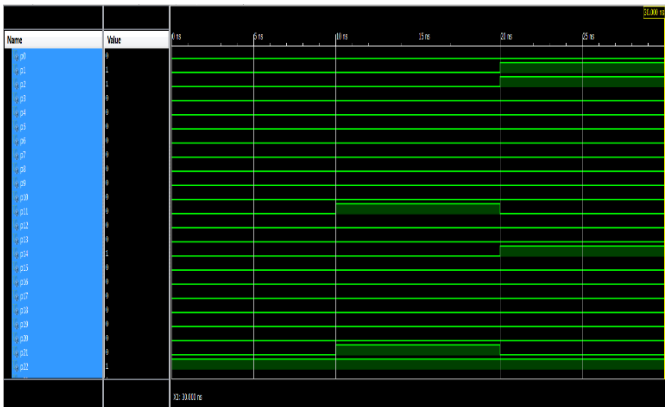

Fig. 10 Simulation Result of 16x16 bit Vedic Multiplier

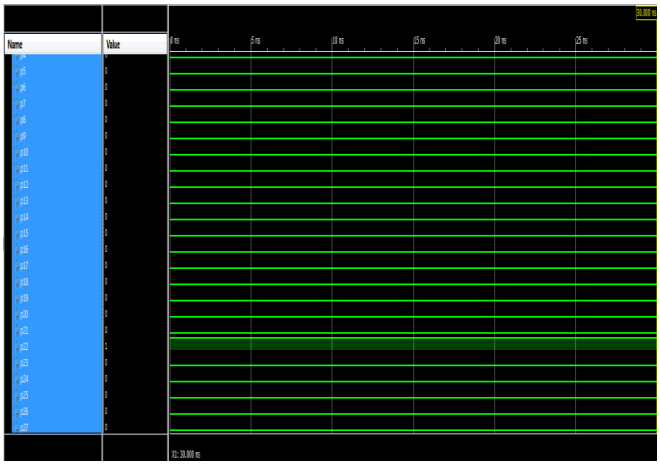

Fig. 11 Simulation Result of 32x32 bit Vedic Multiplier

V.RESULT AND DISCUSSION

The synthesis result obtained from proposed Vedic multiplier is faster than Array and Booth multiplier. The device utilization summary of 8x8 bit Vedic multiplier for Xilinx, Spartan family is shown below:

Device Utilization Summary:

Selected Device:	3s50at q144-5		
Number of Slices:	95 out of	704	13%
Number of 4 input LUTs:	166 out of	1408	11%
Number of IOs:	32		
Number of bonded IOBs:	32 out of	108	29%

In table 1 we can see the comparison between 8x8 bit Conventional multipliers and Vedic multiplier (ours) in terms of computational path delay in nanoseconds (ns). The path delay for 8x8 bit Array and Booth multipliers have been taken from S.S. Kerur et al. [11]. Thus Vedic multiplier has greater advantage as compared to other multipliers in terms of execution time.

Table 1 Comparison of 8x8 bit Multipliers (in ns)

Device: Spartan xc3s50a-5-tq144	Array Multiplier	Booth Multiplier	Vedic Multiplier
Path Delay	32.010 ns	29.549 ns	21.679 ns

Table 2 Comparison of 16x16 bit Multipliers (in ns)

Device: Spartan xc3s50a-5-tq144	Array Multiplier	Booth Multiplier	Vedic Multiplier
Path Delay	64.020 ns	59.098 ns	43.358ns

Table 3 Comparison of 32x32 bit Multipliers (in ns)

Device: Spartan xc3s50a-5-tq144	Array Multiplier	Booth Multiplier	Vedic Multiplier
Path Delay	128.040ns	118.196 ns	86.716ns

VI.CONCLUSION

A highly efficient method of multiplication – "UrdhvaTiryakbhyamSutra" based on Vedic mathematics is presented in this paper. A method for hierarchical multiplier design is given and it clearly indicates the computational advantages offered by Vedic methods. For the proposed 8x8 bit Vedic multiplier the computational delay is found to be 21.679 ns. Thus the delay to be reduced is finely fulfilled. In terms of execution time (speed) Vedic multiplier is much more efficient than Array and Booth multiplier.In future, all the major universities should promote research work in Vedic mathematics by setting up appropriate research centers.

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