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128 BIT SQUARE ROOT CARRY SELECT ADDER

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ABSTRACT

Carry Select Adder is one of the adders used in many data-processing processors to perform arithmetic functions. Carry select adder is used to increase the speed of a parallel adder that expands area in favour of speed.CSLA is used in many computational systems to alleviate the problem of propagation delay by independently generating multiple carriers and then select a carry to generate the sum. The problem raised in CSLA is not area efficient because it uses multiple pairs of Ripple carry adders to generate the partial sum and carry which are selected by the multiplexer.Square Root CSLA is constructed for equalising the delay and area of two carry chains and the block multiplexer signal from previous stage. This is an extension of linear CSLA which improves the delay time greatly. By using SQRT CSLA, the delay and area can be verified, as the time waiting for carry bit is used to calculate an extra input bit in each stage.This modified design will reduce area and delay as compared with regular SQRT CSLA. Based on this modification 8, 16, 32, 64,128-bit SQRT CSLA architecture and simulation will be developed and compare with regular SQRT CSLA.

Index Terms—Keywords:MUX,RCA

I. INTRODUCTION

In the main area of research in VLSI system design, area and power reduction in data path logic systems play a major role. .For high performance processors and systems High-speed addition and multiplication have always been a fundamental requirement.The sum for each bit position in an elementary adder is generated sequentially and a carry propagated into the next position. The circuit architecture is simple and area-efficient. Thus the computation speed is slow because each full-adder can only start operation till the previous carry-out signal is ready.The CSLA is used in many computational systems to moderate the problem of carry propagation delay to generatethe sum. The sum for each bit position in an elementary adder is generated sequentially and a carry propagated into the next position. There are many types of adder designs available, which have its own advantages and disadvantages. The squareroot carry select adder is constructedby equalizing the delay through two carry chains and the block multiplexer signalfrom previous stage.

II. RELATED WORK

2.1 FULL ADDER

Thus the working of a ripple carry adder completely, you need to have a look at the full adder too. Full adder is a logic circuit that adds two input operand bits plus a Carry in bit and outputs a Carry out bit and a sum bit.. The Sum out of a full adder is the XOR of input operand bits A, B and the Carry in bit. Truth table and schematic of a 1 bit Full adder is shown below.There is a simple trick to find results of a full adder. Consider the second last row of the truth table, here the operands are 1, 1, 0 ie (A, B, Cin). Add them together ie 1+1+0 = 10 . In binary system, The number order is 0, 1, 10, 11……. and so the result of 1+1+0 is 10 just like we get 1+1+0 =2 in decimal system. 2 in the decimal system corresponds to 10 in the binary system. Swapping the result “10” will give S=0 and Cout = 1 and the second last row is justified.This can be applied to any row in the table.

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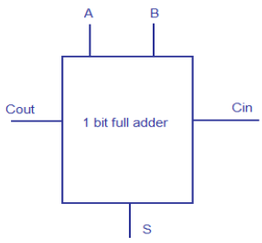
Inputs			Outputs	
A	B	Cin	Cout	S
0	0	0	0	0
1	0	0	0	1
0	1	0	0	1
1	1	0	1	0
0	0	1	0	1
1	0	1	1	0
0	1	1	1	0
1	1	1	1	1



1 bit full adder truth table & schematic

Fig.1. Represent a 1 bit full adder block diagram and truth table.

2.2 RIPPLE CARRY ADDER

Ripple carry adder circuits can be cascaded in parallel to add an N-bit number. For an N- bit parallel adder, there must be N number of full adder circuits. A ripple carry adder is a logic circuit in which the carry-out of each full adder is the carry in of the succeeding next most significant full adder. In this adder the sum and carry out bits of any half adder stage is not valid until the carry in of that stage occurs.Propagation delays inside the logic circuitry is the reason behind this. Propagation delay is time elapsed between the application of an input and occurance of the corresponding output. The time taken for the NOT gateoutputto the NOT gate input is the propagation delay here. Similarly the carry propagation delay is the time elapsed between the application of the carry in signal and the carry out signal.

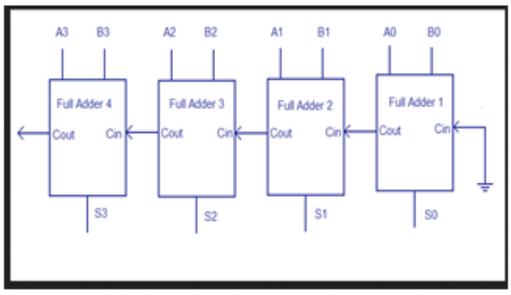


Fig.2. Represent a 4 bit ripple carry adder block diagram.

III. LOGIC FORMULATION

The basic CSLA combination of two n-bit RCAs called as sum and carry generating unit (SCG), and sum and carry selection unit (SCS) [9]. SCG unit takes most of the logic resources and it contributes major role in critical path. Different methods are proposed for optimized SCG unit. It is studied that the logic design of the SCG unit [6]. The main motto for this study is to identify the redundant logics operations and data dependence, then eliminating all the redundant operations and sequential operations.

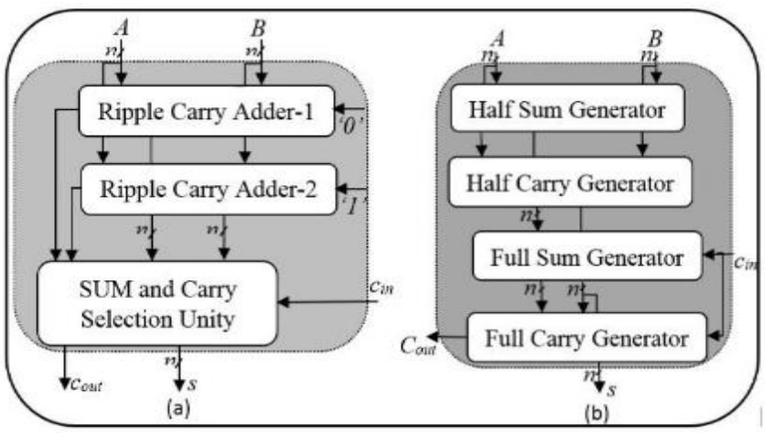


Fig. 3. Logic Block Diagram of: (a) Conventional Carry Selector Unit, and (b) Ripple Carry Adder

RCA block has these four sub-blocks: half sum generator (HSG) unit, half carry generator (HCG) unit, full sum generator (FSG) unit and full carry generator (FCG) unit. The HSG block generates sum and carry output using the conventional half adder circuit using the corresponding bits of the CSLA. It consists of N numbers of XOR gates and AND-gates to perform the operation.

IV.PROPOSED SYSTEM

16-bit sqrt carry select adder

A 16 bitsqrtcarry-select adder is divided into sectors, each of which, except for the least significant performs two additions in parallel, one assuming a carry-in of zero, the other a carry-in of one within the sector, there are two 4-bit rca receiving the same data inputs but different Cin.

The actual Cin from the preceding sector selects one of the two adders. If the carry-in is zero, the sum and carryout of the upper adder are selected. If the carry-in is one, the sum and carry-out of the lower adder are selected. The structure of regular 16-bit SQRT CSLA has five groups of different size RCA as shown in figure 4.

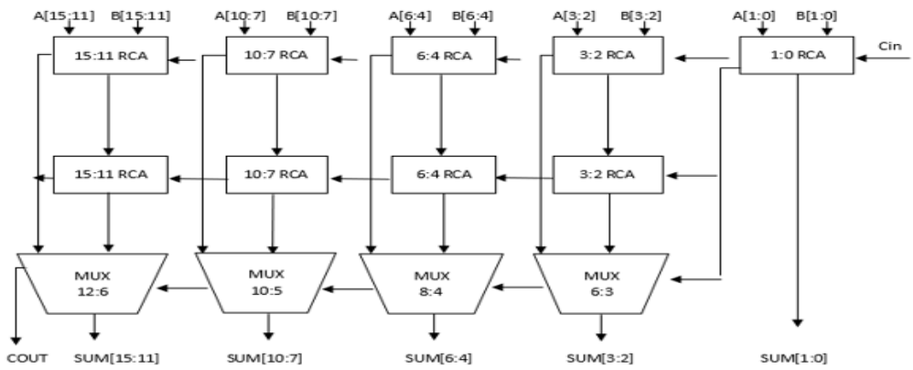
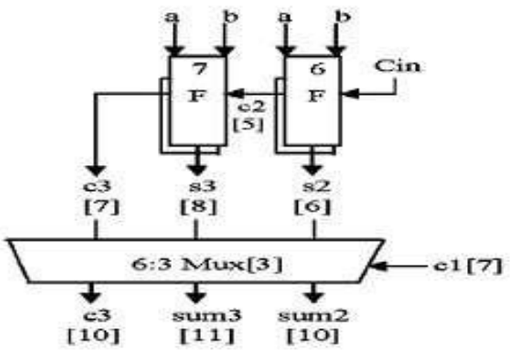
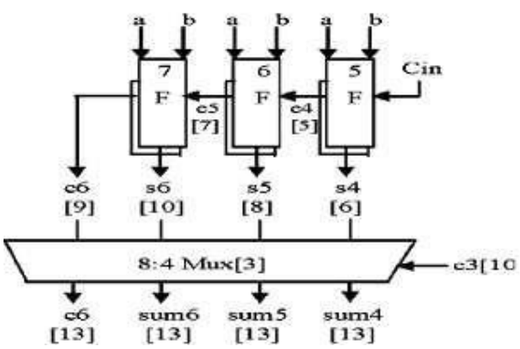


Fig. 4. Regular 16-b SQRT CSLA



(a)



(b)

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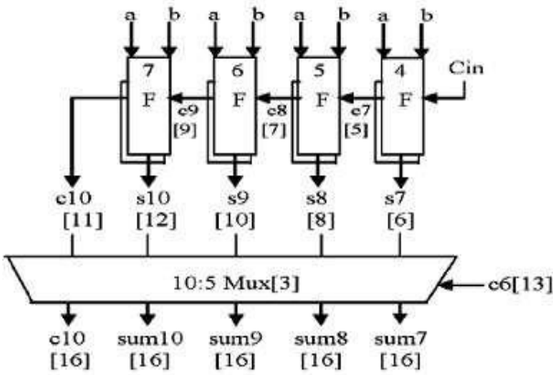
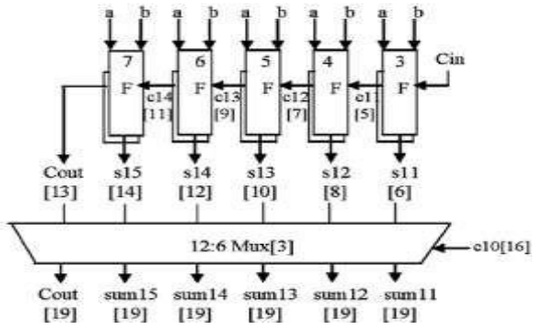
A carry-select adder achieves speeds 40% to 90% faster by performing additions in parallel and reducing the maximum carry path.



(c)



(d)

Delay and area evaluation of regular SQRT CSLA: (a) group2, (b) group3, (c) group4, and (d) group5. F is a Full Adder.The delay and area evaluation of each group are shown in Fig. 4, inwhich the numerals within [] specify the delay values, e.g., sum2 requires 10 gate delays.

V. COMPARISON OF REGULAR AND MODIFIED 128 – BIT CSLA

Comparison of Regular and modified 128-bit CSLA. The delay overhead for the 8, 16, and 32-b is 14%, 9.8%, and 5.63% respectively, whereas for the 64-b it reduces to only 4.75%. The power–delay product of the proposed 8-b is higher than that of the regular CSLA by 5.2% and the area -delay product is lower by 2.9%. However, the power-delay product of the proposed 16-b CSLA reduces by 1.76% and for the 32-b and 64-b by as much as 8.18%, and 12.28% respectively. Similarly the area-delay product of the proposed design for 16-bit, 32-bit, 64-bit and 128-bit is also reduced by 6.7%, 11%, and 14.4% respectively.

Adders		Delay(ns)	Area(μm^2)
32-bit	Regular	20.96	90
	Modified	15.63	87
64-bit	Regular	33.85	189
	Modified	29.75	186
128-bit	Regular	42.36	439
	Modified	36.52	431

Fig.5. Represent a comparison table of regular and modified 128-bit csla.

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VI.RESULT ANALYSIS

The implemented design in this work has been simulated using Verilog-HDL (Modelsim). The adders 128 BIT are designed and simulated using Modelsim. After simulation the different size codes are synthesized using Xilinx ISE 10.1. The simulated files are imported into the synthesized tool and corresponding values of delay and area are noted. The synthesized reports contain area and delay values for SQRT root CSLA.

VII.SIMULATIONS

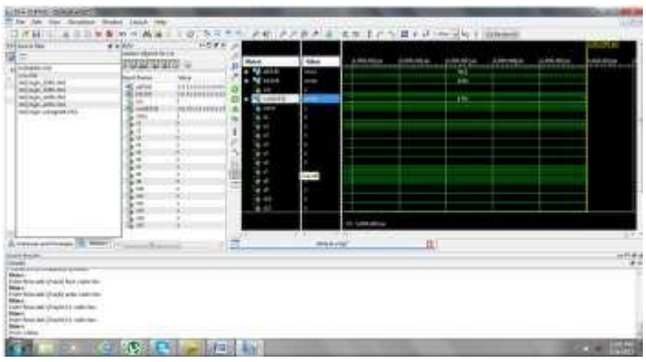

Fig.6.Represent Thus the simulation results for the 16 bit SQRT CSLA is depicted below using Xilinx software.

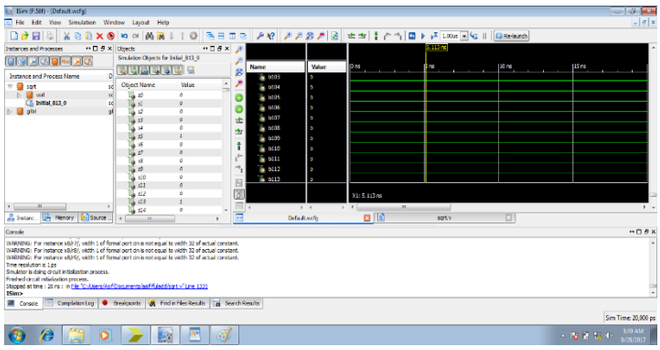

Fig.7.Represent Thus the simulation result for the specified 128 bit SQUARE ROOT CARRY SELECT ADDER is depicted below Xilinx software.

VIII. CONCLUSION AND FUTURE SCOPE

This work present Efficient Architecture of modified linear Carry Select Adder simple approach to reduce the area and delay. Design by SQUARE ROOT CSLA architecture. We had compared the working of two SQRT CSLA by implementing each of them separately using RCA and MUX. In this adder, it accomplishes the addition by adding small portions of bits then it selects the correct outputs using multiplexer.

The conventional carry select adder has the disadvantage of more power consumption and occupying more chip area. The proposed CSLA using common Boolean logic has low power and less delay. The reduced number of gate of this work offers the great advantage in the optimisation of area and total power. The SQRT CSLA using MUX can be in many processing processors in order to achieve fast performance. The Area and Power can be reduced. We also conclude that this addition technique can be implemented for larger higher values of bits.

REFERENCES

[1] BehnamAmelifard, FarzanFallah and MassoudPedram, “Closing the gap between Carry Select Adder and Ripple Carry Adder: a new class of low-power high-performance adders”, Sixth International Symposium on Quality of Electronic Design, pp.148-152. April 2005.

[2] B. Ramkumar, H.M. Kittur, and P. M. Kannan, ―ASIC implementation of modified faster carry save adder,‖ Eur. J. Sci. Res., vol. 42, no. 1, pp. 53–58, 2010.

[3] J. M. Rabaey, Digtal Integrated Circuits—A Design Perspective. Upper Saddle River, NJ: Prentice-Hall, 2001.

[4] Y. He, C. H. Chang, and J. Gu, ―An area efficient 64 -bit square root carry-select adder for low power applications,‖ in Proc. IEEE Int. SympCircuits Syst., 2005, vol. 4, pp. 4082–4085.

[5] KuldeepRawat, TarekDarwish. andMagdyBayoumi, "A low power and reduced area Carry Select Adder", 45th Midwest Symposium on Circuits and Systems, vol.1, pp. 467-470,March 2002.

[6] M.Moris Mano, "Digital Design", Pearson Education, 3rd edition, 2002.

[7] Youngjoon Kim and Lee-Sup Kim, "A low power carry select adder with reduced area", IEEE International Symposium on Circuits and Systems, vol.4, pp.218-221, May 2001.

[8] Youngjoon Kim and Lee-Sup Kim, "64-bit carry-select adder with reduced area", Electronics Letters, vol.37, issue 10, pp.614-615, May 2001.

[9] " Design compiler User Guide " ver.B-2008.09, Synopsys Inc., Sep.2008.

[10] C.Cheng and K.K.Prathi, ―Furthur complexity reduction of parallel FIR filters,‖ in Proc.IEEEInt.Symp.circuitssyst.Kobe, Japan, May 2005.