Non Redundant Radix-4 Signed Digit encoding DSP Accelarator

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ABSTRACT

Dsp accelerator has very prominent role in digital signal processing applications. Accelaration mainly performed in the application specific integrated circuit devices. Dsp accelator has perform various arithmetic operations to improve the performance of the accelation proposed technique is implemented i.e NR4SD.i.e.Non Redundant Radix-4signed digit encoding technique, it has high performance compared with the modified booth algorithm and also it has lass decoding time for data transmission.In this paper the complete design of dsp acclelator is designed with NR4SD technique to improve the area, delay and power concumption. It has implemented with the verilog hdl and synthesize and simulated with the XILINX 14.5 ISE standard.

Keywords: NR4SD, Pre encoded multiplier, FCU, carry save form, modified booth encoding.

I. INTRODUCTION

Modern embedded systems target high-end application do-mains requiring economical implementations of computationally intensive digital signal process (DSP) functions. The incorporation of heterogeneity through specialised hardware accelerators improves performance and reduces energy consumption. Although application-specific integrated circuits (ASICs) kind the perfect acceleration solution in terms of performance and power, their inflexibility leads to magnified atomic number 14 quality, as multiple instantiated ASICsare required toaccelerate varied kernels. several researchers have proposed the utilization of domain-specific coarse-grained reconfigurable accelerators so as to extend ASICs' flexibility while not significantly compromising their performance.

Highance versatile datapathshavebeen projected to expeditiously map primitive or enchained operations found within the initial data-flow graph (DFG) of a kernel. The templates of complicated enchained operations area unit either extracted directly from the kernel's DFGor laid out in a prede-fined activity templet librar. style selections on the accelera-tor's datapath highly impact its potency. Existing works on coarse-grained reconfigurable datapaths in the main exploit architecture-level optimizations, e.g., magnified instruction level correspondence (ILP)

Thedomain specific design generation algorithms of vary the type and variety of computation units achieving a custom-made design structure. In, versatile architectures were projected exploiting ILP and operation chaining. Recently, Ansaloni et al. Adopted aggressive operation chaining to change the com-putation of entiresubexpressions mistreatment multiple ALUs with heterogeneous arithmetic options. The said reconfigurable architecture-

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sexcludearithmeticoptimiztions throughout the field of study synthesis and consider them solely at the interior circuit structure of primitive components, e.g., ad-ders, through-out the logic synthesis.

However, research activities have shown that the arithmetic optimizations at higher abstraction levels than the structural circuit one considerably impact on the datapath performance. In, timing-driven optimizations supported carry-save (CS) arithmetic were performed at the post-Register Transfer Level (RTL) style stage. In, common subexpression elimination in metal computations is employed to optimize linear DSP cir-cuits. Verma et al. developed transformation techniques on the application'sDFG tomaximise .

The utilization of metal arithmetic previous the actual datapath synthesis. The said metal improvement approaches target inflexible datapath, i.e., ASIC, implementations. Recently, Xydis et al. projected a versatile design combining the ILP and pipelining techniques with the CS-aware operation chaining. However, all the said solutions feature an inherent limitation, i.e., metal improvement is finite tomergingonlyaddi-tions / subtractions.

A metal to binary conversion is inserted before every operation that differs from addition/subtraction, e.g., mul-tiplication, thus, allocating multiple metal to binary conversions that heavily degrades performance owing to long carry propagations. In this transient, we have a tendency to propose a superior field of study theme for the synthesis of versatile hardware DSP accel-erators by combining optimization techniques from each the design and arithmetic levels of abstraction. we have a tendency to introduce a versatile datapath design that exploits metal optimized templates of enchained operations. The projected architecture includes versatile procedure units (FCUs), which enable the execution of an outsized set of operationtemplatesfoundinDSPkernels.

II. MODIFIED BOOTH ALGORITHM

Modified booth algorithm is used for signed digit multiplication, both A and B variable consist n=nk bits and B represented as in th modified booth form that is dhown in below.

$$B = \langle b_{n-1} \ldots b_0 \rangle_{2's} = -b_{2k-1}2^{2k-1} + \sum_{i=0}^{2k-2} b_i 2^i$$

$$= \langle \mathbf{b}_{k-1}^{MB} \ldots \mathbf{b}_0^{MB} \rangle_{MB} = \sum_{j=0}^{k-1} \mathbf{b}_j^{MB} 2^{2j}.$$

B is formed with in the limits of {-2,-1,0.1,2},and

$$\mathbf{b}_j^{MB} = -2b_{2j+1} + b_{2j} + b_{2j-1}, \tag{2}$$

So, B is devided into three digit set like b_{2j-1},b_{2j},b_{2j+1},it can be denoted as signed bits depends on MSB bits, each set has individual operation that has shoen in below table:

TABLE 1
Modified Booth Encoding

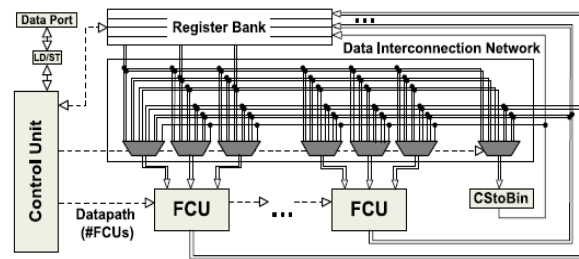| b_{2j+1}	b_{2j}	b_{2j-1}	$\mathbf{b}_j^{MB}$	s_j	one_j	two_j
0	0	0	**0**	0	0	0
0	0	1	**+1**	0	1	0
0	1	0	**+1**	0	1	0
0	1	1	**+2**	0	0	1
1	0	0	**−2**	1	0	1
1	0	1	**−1**	1	1	0
1	1	0	**−1**	1	1	0
1	1	1	**0**	1	0	0

Fig. 1. Abstract form of the flexible datapath.

III. PROPOSED FLEXIBLE ACCELERATOR

The projected versatile accelerator design is shown in Fig. 1. Each FCU operates directly on metal operands and produc-es knowledge in the same form1 for direct use of intermediate results. Each FCU operates on 16-bit ope-rands.

Such a bit-length is adequate for the most DSP datapaths, however the field of study construct of the FCU can be foursquare custom-made for smaller or larger bit-lengths. The number of FCUs is decided at style time sup-ported the ILP and space constraints obligatory by the designer. The CStoBin module could be a ripple-carry adder and converts the metal kind to the two's complement one. The register bank consists of scratch registers and is used for storing intermediate results and sharing operands among the FCUs. completely dif-ferent DSP kernels (i.e., completely different register allocation and electronic communication patterns per kernel) is mapped onto the projected design mistreatment post-RTL datapath interconnection sharing techniques. The management unit drives the architecture (i.e., communication between the in-fo port and also the register bank, configuration words of the FCUs and choice signals for the multiplexers) in every clock cycle.

IV. NON REDUNDANT RADIX4 SIGNED DIGIT ENCODNG

In this section Non redundant radix-4 signed digit encoding has represented, which is advanced method to the modified booth algorithm technique. Modified booth algorithm has worked for the moduli set {-2,-1,0,1,2} but this proposed technique has devided into NR4SD+ and NR4SD- with respect to {-2,-1,0.1} and {-1,0.1,2} moduli sets.

The proposed FCU is designed with the NR4SD techniques to improve the performance.The block diagram of proposed multipler with NR4SD is shown in the below figure:
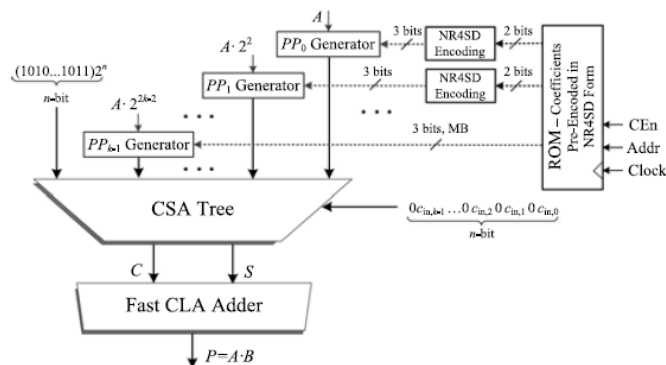
The above diagram represents the proposed multiplier with NR4SD technique, in this the variable B has devided intothe sets this are initially stored in the memory ROM. These bits are nothing but n^-_{2j+1}, n^+_{2j} for NR4SD+ and n^+_{2j+1}, n^-_{2j} for NR4SD-.

Thes eimplementations are shown in the belof figure.

(a)

(b)
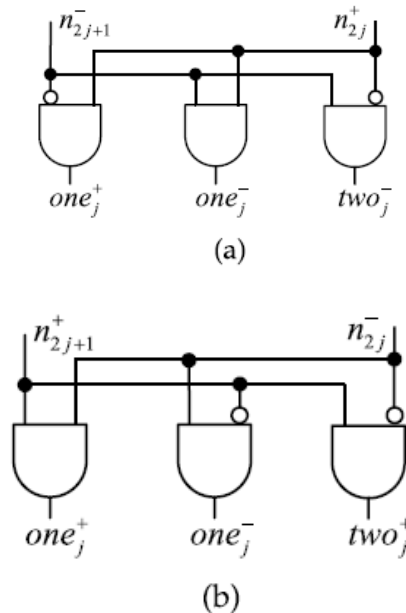
From the bits of n^-_{2j+1}, n^+_{2j} and n^+_{2j+1}, n^-_{2j} ,three moduli bits are generated one^+j, one^-j, two^-j and one^+j, one^-j, two^-j , these are shown in the above diagram. From these the required partial products PP bits are generated as shown in the below figures for NR4SD+ and NR4SD-.

(e) (f)
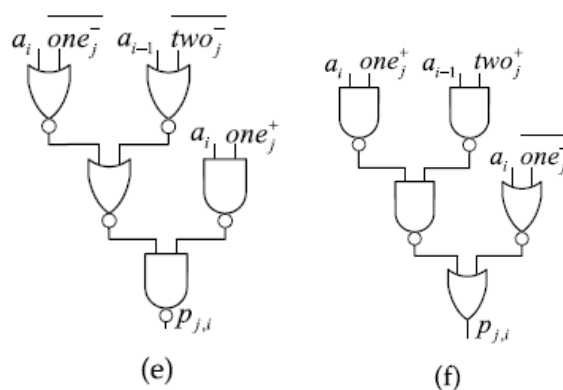
IV. IMPLEMENTATION RESULTS

We executed in Verilog the multiplier plans of Table 5.The PPGs for the NR4SD , NR4SDþ multipliers (Figs. 4c and 4d, separately) contain countless since all the A bits are supplemented if there should arise an occurrence of a negative digit. In request to maintain a strategic distance from these inverters and, in this way, diminish the territory/ control/deferral of NR4SD , NR4SDþ pre-encoded multipliers, the PPGs for the NR4SD , NR4SDþ multipliers were outlined in view of primitive NAND and NOR entryways, and supplanted by Figs. 4e and 4f, separately. The CSA tree and CLA snake were transported in from Synopsys. DesignWare library. The ROM

for the 2's supplement or preencoded coefficients is a synchronous ROM of 512 words regularly met at DSP frameworks, e.g., discourse CoDecs or sound sifting [20]. The width of every ROM relies on upon the multiplier engineering (Table 5). A limited state machine synchronized the information stream and the multiplier operation yet was not considered in the region/control figurings.

V. SYNTHESIS AND SIMULATION RESULTS

In this paper the new design NR4SD technique is used to design the FCU unit for DSP acclelarator and its implemented with the XILINX ISE 14.5 simulation tool and implemented with Verilog HDL. The RTL diagram and simulation results are displayed below.
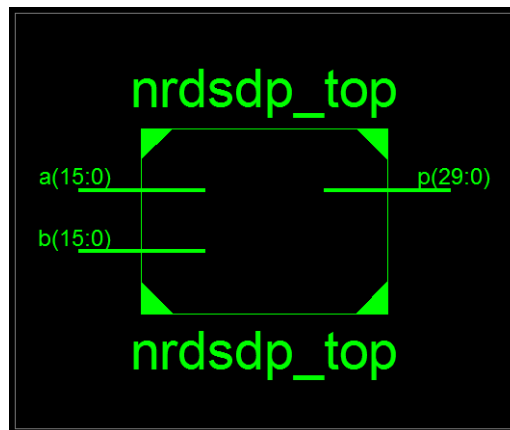

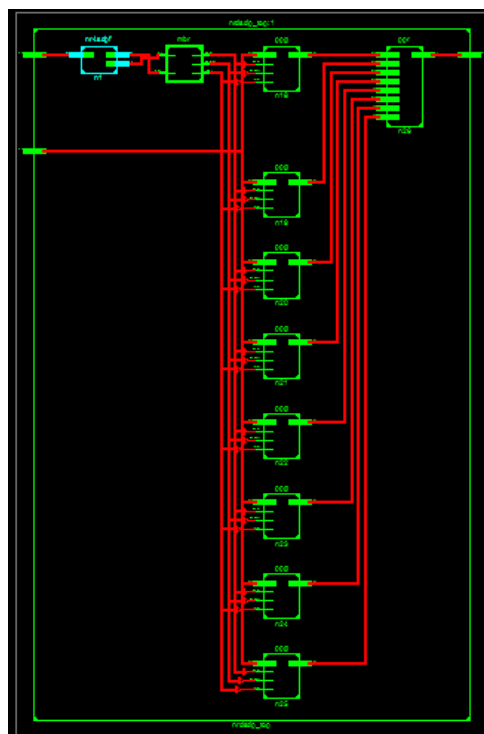**Fig: Top level schematic diagram**

Fig: Internal architectures of RTL diagram

Synthesis result:

Proposed NR4SD based FCU unit results:

| Device Utilization Summary (estima	
Logic Utilization	**Used**
Number of Slice LUTs	166
Number of fully used LUT-FF pairs	0
Number of bonded IOBs	158

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Total            13.651ns (3.052ns logic, 10.599ns route)
                 (22.4% logic, 77.6% route)
```

MB based FCU unit results:

Device Utilization Summary (estima	
Logic Utilization	**Used**
Number of Slice LUTs	311
Number of fully used LUT-FF pairs	0
Number of bonded IOBs	62

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-----------------------------------------
Total            14.665ns (2.135ns logic, 12.530ns route)
                 (14.6% logic, 85.4% route)
```

Simulation result:
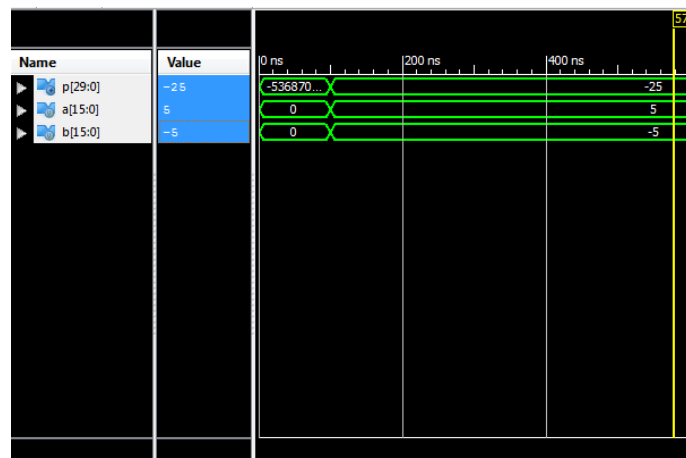
VI. CONCLUSION

In this paper it consist the design of flexible unit with non redunadant radix-4 sign encoding technique for DSP acclearator unit. It performs several arithmetic operations, the experimental results shows the proposed FCU unit has better performance compared with the MB encoding based FCU unit with the area and delay.

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