DEVELOPMENTOF A DIGITALLY TUNED QUADRATURE OSCILLATOR

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ABSTRACT

In this research paper,a digitally tuned quadrature oscillator has been designedand simulated which provides the facility of tuning the frequency of oscillationsdigitally having good linearity with digital control word. Now a days, digitally tuned devices are very useful because hybrid systems (i.e., a combination of analog & digital systems) are preferred due to the advances in IC technology to obtain the advantages of both the analog and digital world. This type of digitally tuned quadrature oscillator will be very attractive from the point of view of interfacing. Here, the wide range of the frequency of oscillations for oscillator circuit can be achieved which is controlled by a digital control word (n-bit long). The main aim of designing the oscillator circuit is for synthesising the frequency hopping signals used inindirect method of frequency hopping spread spectrum. In order to perform the software implementation of this oscillator, PSPICE simulation tool on Windows platform has been used withconforming results in support of the theory. The density and speed of N-MOSFETs are very high that's why thesetransistors have been used for switching purpose.

Keywords:Positive feedback; Digitally-tuned, R-2R Ladder Network; Quadrature Oscillator; Frequency of oscillations.

I. INTRODUCTION

The oscillators with only RC components are preferred for a range of frequencies (especially from low to medium) because they can be fabricated and integrated easily and physically use very small area as compared to other realizations [1]. A sinusoidal quadrature oscillator is a circuit that provides two sinusoids with 90^0phase difference at the same time and can be used in a variety of applications, such as in telecommunications for quadrature mixers, in single-sideband generators, and in direct-conversion receivers or for measurement purposes in vector generators/ selective voltmeters [2]. Basically, the sinusoidal quadrature signalsare fundamental need of modern RF-communication systems such as zero-intermediate frequency and image-reject receivers [3].Many multiphase oscillator circuits using operational amplifiers (Op-Amps) have been proposed but none of these provides the sinusoidal quadrature output voltages [4–6]. A quadrature oscillator circuit with orthogonally controllable oscillation frequencies using Op-Amps has been developed which provides two sinusoidal signalsbut lacking the programmability feature [7]. At present, there is a great interest in developing the digitally tuned analog signal processing circuits. These digitally tuned devices have become attractive for mixed digital–analog applications. In particular, digital tuning of analog oscillators improves system flexibility, economy, and performance of the system in several applications [8-11]. The oscillators based on operational transconductance amplifier (OTA) providedthe facility of electronic tuning but suffered from linearity problems. A new technique of designing sinusoidal oscillators based on the digitally tuned current follower and voltage

follower was proposed which provided the advantage of digital programmability and high-frequency operation while offering better linearity but could not provide the quadrature output voltages [12].

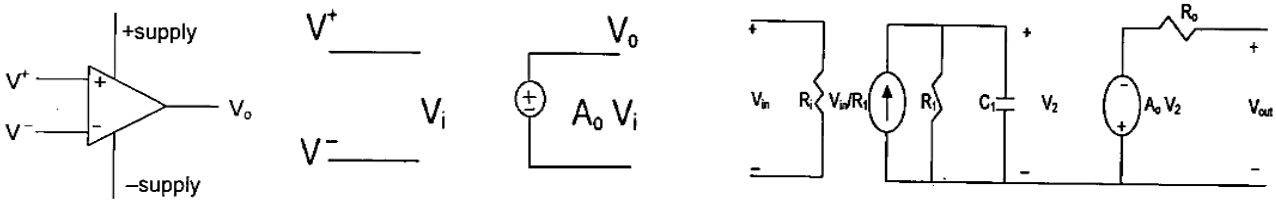
In this research paper, a new improved version of digitally tuned quadrature oscillator using Op-Amps has been designed and results have been verified by simulation tool PSPICE on Windows platform, which results in simplicity, low cost, lower output impedance, and higher current driving capability. In mixed analog/digital systems, the digitally tuned feature of the proposed approach allows us to interface directly with the digital signal processing unit. Most of the modern systems utilize digital signal processing unit to adapt the parameters of an oscillator with additional minimum hardware and cost.The main aim of designing thisdigitally tunedoscillator circuit is for generating the frequency hopping signals used inindirect method of frequency hopping spread spectrum system.

II. BASIC BUILDING BLOCKS USED IN QUADRATURE OSCILLATOR CIRCUIT

Before going into the detailed discussion of the circuit diagrams for the digitally tunedquadrature circuit, it is better to discuss the various building blocks or sub-circuits which are used in the design and simulation of the circuit underconsideration.

2.1 OPERATIONAL AMPLIFIER (OP-AMP)

An Op-Amp is a direct coupled differential amplifier with very high gain A_o (typically $A_o>10^5$) at low-frequencies. Generally, Op-Amps are used with external feedback to control gain-bandwidth productand to stabilizethe extremely large variability of the Op-Amp parameters.Currently, Op-Amps are available in all semiconductor integrated circuit processing techniques (bipolar, NMOS, PMOS, CMOS, GaAs), so the circuits can be designed which are compatible with the technology of choice. The symbol, small signal equivalent circuit of an ideal Op-Amp and its linear ac model with a single break frequency are shown in figure (1).This model does not take into account the saturation effect and is suitable only if an op-amp operates within the linear region [13-14].



(a) Circuit Symbol (b) Small Signal Model (c) Linear AC Model

Fig. (1) Operational Amplifier (Op-Amp)

2.2 DIGITAL CONTROLLER USING R-2R LADDER NETWORK

Here, an R-2R ladder network is used for digital to analog conversion. The value in digital code (such as straight binary or BCD) can be converted to its proportional voltage or current and this converted value is discrete in nature too. However, if the step size taken is small, it may be considered as continuous quantity with better resolution [15]. The circuit diagram of R-2R ladder network is shown in figure (2) and the block diagram of D/A converter (DAC) is shown in figure (3) [16].

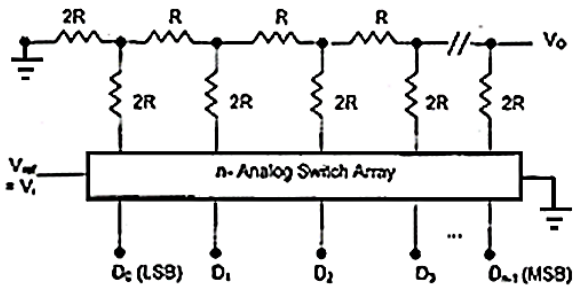


Fig. (2) n-bit R-2R Ladder Network

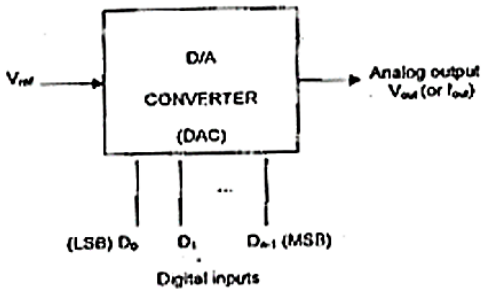


Fig. (3) Block Diagram of n-bit Digital to Analog Converter

Generally, the digital inputs are derived from the output register of a digital system. There are n-bits D_0, D_1, ..., D_{n-1} and reference voltage, V_{ref} which determine the value of output voltage or current. Here, the output voltage can be defined as [17-18]:

$$V_o = (D_0 + 2^1 D_1 + 2^2 D_2 + \cdots + 2^{n-1} D_{n-1}) V_{ref} / 2^n$$

$$\Rightarrow \quad V_o = (N/2^n) V_{ref} \qquad (1)$$

where, $N = (D_0 + 2^1 D_1 + 2^2 D_2 + \ldots\ldots + 2^{n-1} D_{n-1})$ is the digital control word.

2.3 1/2-STAGE R-2R LADDER NETWORKS

As observed from the expression of equation (1), the output is proportional to the control word (N) in 1-stage R-2R ladder network circuit and is represented by K_1. The value of K_1 is given as[17-18]:

$$K_1 = \frac{N}{2^n} \qquad (2)$$

Thus, the output of the 1-stage R-2R ladder circuit is:

$$V_o = K_1 V_{ref} \qquad (3)$$

The block diagram of the 1-stage R-2R ladder network is shown in figure (4a), whose transfer function is given by K_1, and $K_1 = (V_o / V_{ref})$.

The 2-stage R-2R ladder network consists of two 1-stage R-2R ladder networks in cascade, which are connected through a buffer. The same control word (N) is fed to both K_1-blocks. The block diagram representation of the 2-stage ladder network (K_2) is illustrated in figure (4b) and its output is given by:

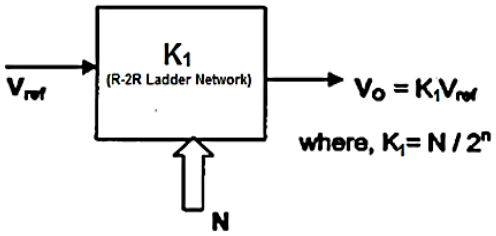
$$V_o = K_1 . K_1 V_{ref} = K_1^2 V_{ref}$$

or, $$V_o = K_2 V_{ref} \qquad (4)$$

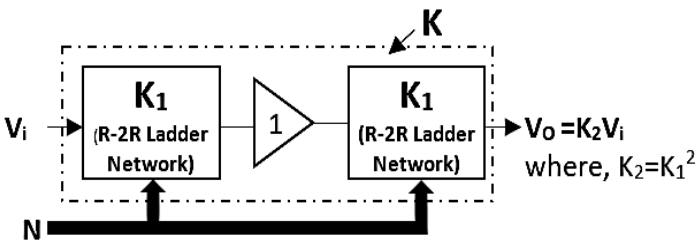
where, $$K_2 = K_1^2$$

$$\Rightarrow \quad K_2 = (N/2^n)^2 \qquad (5)$$

Therefore, the transfer function of this 2-stage ladder circuit is simply K_2.



(a) One stage R-2R Ladder Network



(b) Two stage R-2R Ladder Network

Fig. (4) Block Diagrams of R-2R Ladder Networks

2.4R-2R LADDER NETWORK DRIVEN BY DIGITAL INPUT

The analog switches are fed by the digital inputs generated by a digital system (register outputs) which in turn switch the signal levels at the input of 2R resistors of the ladder network. An analog switch arrayshown in figure (5)is made up of NMOS transistors &CMOS inverters and it is also used as an interface between R-2R ladder network and the output register of a digital system[19].

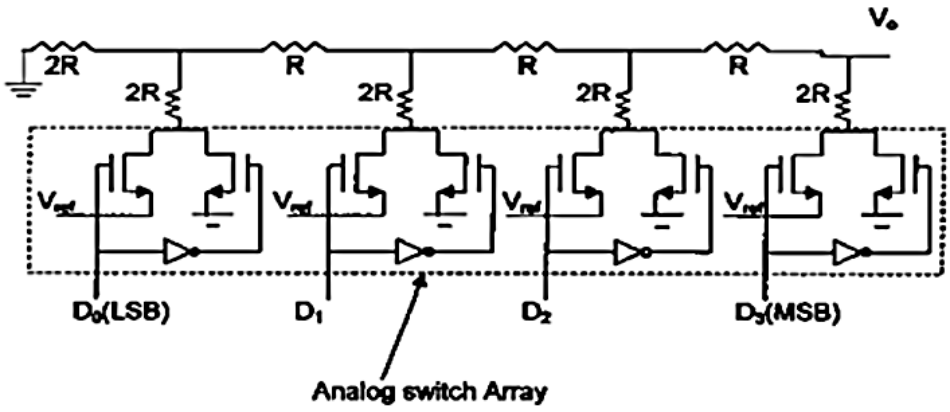


Fig. (5) R-2R Ladder Network driven by Digital Control Word

In this work, R-2R ladder network is designed especially for only 4-bits but it can be extended for n-bits by simply adding the R-2R resistances in parallel within the ladder network. The main purpose of analog switch array is to connect 2R resistor conditionally either to the reference input (V_{ref}) or ground basedon the status of the bits in the digital control word. If the particular bit is high, the 2R resistor is connected to V_{ref}. On the other hand, the 2R resistor is connected to ground if the bit is lowbecause one NMOS is ON and other will be OFF at that moment. A number of switches may be used here but NMOS transistors are more suitable because they have constant ON resistance in the ohmic region and the ON-resistance of NMOS transistor gets added with 2R resistance. In both the cases (the control bit is 0 or 1), the added resistance with 2R is same, i.e., the ON-resistance of the NMOS transistor. Here, the gate to source voltage is greater than the threshold voltage of the NMOS transistor. If it is not so, then the transistor will not operate in the ohmic region. It must also be taken into account that the ratio of the resistors (i.e., 2R/R = 2) in the ladder circuit must remain constant which is equal to 2. To ensure the operation of NMOS transistor in ohmic region, the value of V_{ds} must bevery small in comparison to the value ofV_{gs} and the value of ON-resistance of the NMOS may be given as [20-21]:

$$R_{ON} = \frac{L}{W K'_N (V_{gs} - V_t)}; (V_{gs} - V_t) > 0, V_{ds} < (V_{gs} - V_t) \quad (6)$$

where, L is the channel length, W is the width of the channel and K'_N = 2.5 x 10^{-5} A/V^2 is transconductance parameter. In this particular work, the values of L and Ware selected such that the R_{ON} is of 1kΩ. If V_{gs}= 5V and V_t = 1V, then W/L ratio from equation (6) comes out to be 10.

III. DESIGNING OF QUADRATURE OSCILLATOR CIRCUIT

3.1 DESIGNING& ANALYSIS OF SINUSOIDAL QUADRATURE OSCILLATOR CIRCUIT

An amplifier withpositive feedback whose magnitude of closed loop gain (|Aβ|)is greater than unity and at the same time fulfils the phase conditions is called an oscillator circuit. If the output signal of the circuit varies sinusoidally then it is referred to as a sinusoidal oscillator. The Barkhausen criterion for sinusoidal oscillations is stated below:

(i) The magnitude of the closed loop gain, |Aβ|must be unity

(ii) The phase shift through the amplifier and feedback network is 2πn radians, where 'n' is an integer

Thus, the Barkhausen criterion is equivalent to stating that both the phase margin and gain margin are zero. In every practical oscillator circuit, the closed loop gain is slightly larger than unity and the amplitude of the oscillations is limited by the onset of non-linearityof the output of the circuit.

The quadrature oscillator circuit shown in figure (6) is made up of two integrator loops in which the first Op-Amp(OA1) is used in inverting mode called an inverting Miller integrator and the second Op-Amp (OA2) is employed in non-inverting mode called a non-inverting integrator. It provides two sinusoids having a phase difference of 90°, thus,the name given to it isquadrature oscillator circuit. The analysis of this circuit for the calculation offrequency of oscillations [22] is given below.

The transfer function of first op-amp, OA1 is given by:

$$T_1(s) = -\frac{1}{sC_2R} \tag{7}$$

The transfer function of second op-amp, OA2 is given as:

$$T_2(s) = \frac{R_4(R_1+R_2)}{sC_1R_1R_3R_4+(R_1R_4-R_2R_3)} \tag{8}$$

According to condition of oscillations, the closed loop gain must be unity, i.e.,$T_1(s)T_2(s) = 1$

$$\text{Therefore,} -\frac{1}{sC_2R}\cdot\frac{R_4(R_1+R_2)}{sC_1R_1R_3R_4+(R_1R_4-R_2R_3)} = 1$$

$$\Rightarrow \quad s^2 + \frac{R_1R_4-R_2R_3}{C_1R_1R_3R_4}s + \frac{R_1+R_2}{C_1C_2R_1R_3R} = 0 \tag{9}$$

Thus, the condition of oscillations is found by equating the coefficient of `s' equal to zero in equation (9) which is given below:

$$\frac{R_1R_4-R_2R_3}{C_1R_1R_3R_4} = 0$$

$$\Rightarrow \quad R_1/R_2 = R_3/R_4 \tag{10}$$

The frequency of oscillations is obtained by the following expression:

$$w_o = \left[\frac{R_1+R_2}{C_1C_2R_1R_3R}\right]^{1/2}$$

$$\Rightarrow \quad f_o = \frac{1}{2\pi}\left[\frac{R_1+R_2}{C_1C_2R_1R_3R}\right]^{1/2} \tag{11}$$

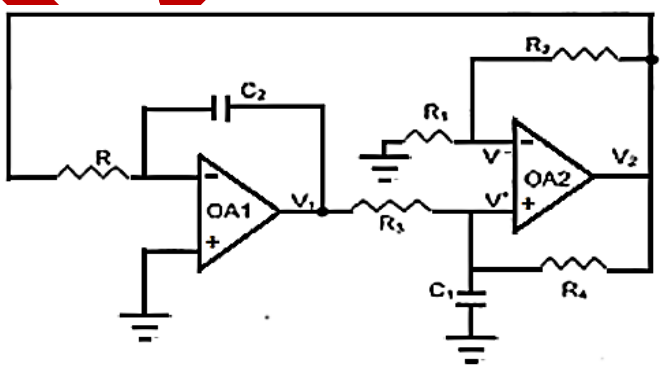


Fig. (6) Basic Quadrature Oscillator Circuit

3.2 DESIGNING OF DIGITALLY TUNED QUADRATURE OSCILLATOR CIRCUIT

The basic circuit of quadrature oscillator given in figure (6)can be made digitally tuned by simply cascading K_2-block (succeeded by a buffer) with resistor (R) as shown in figure (7).The frequency of oscillations for the digitally tuned quadrature oscillator is found to be:

$$f_o = \frac{1}{2\pi}\left[\frac{K_2(R_1+R_2)}{C_1C_2R_1R_3R}\right]^{1/2}$$

where, $K_2 = (N/2^n)^2$. Now, the frequency of oscillations (f_o) becomes:

$$f_o = \frac{1}{2\pi}\left[\left(\frac{N}{2^n}\right)^2 \frac{(R_1+R_2)}{C_1C_2R_1R_3R}\right]^{1/2}$$

$$\Rightarrow \quad f_o = \frac{1}{2\pi}\left(\frac{N}{2^n}\right)\left[\frac{R_1+R_2}{C_1C_2R_1R_3R}\right]^{1/2} \qquad (12)$$

Equation (12) depicts that by simply varying the digital control word (N),the frequency of oscillations can belinearlytuned. Thus, such types of digitally tuned oscillators are very much useful in the area of secure communication which usesfrequency hopping technique of spread spectrum system where the frequency of carrier signal hops for every bit duration of transmission.

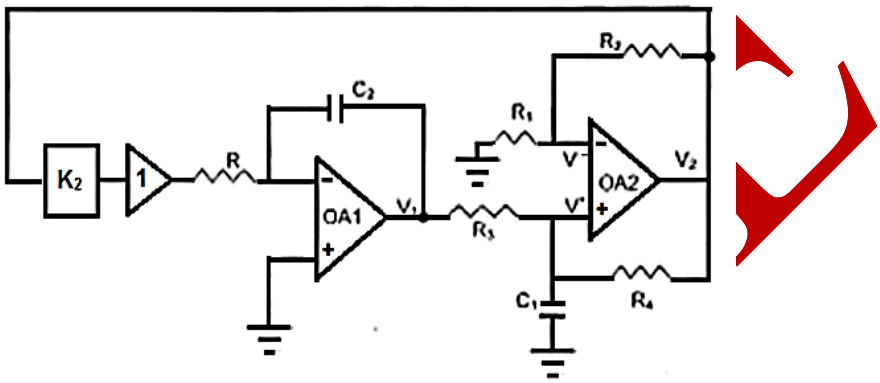


Fig. (7) Digitally Tuned Quadrature Oscillator Circuit

IV. SIMULATION RESULTS & DISCUSSION

In order to perform the validation of the proposed scheme, the circuit for digitally tuned oscillator based on 2-stage R-2R ladder network is simulated using PSPICE [23] simulation tool. For the following resistive and capacitive components: R = 10 kΩ, $R_1 = R_2 = R_3 = R_4 = 20$ kΩ, and $C_1 = C_2 = 0.9947$ nFused in the circuit of figure (7), the frequency of oscillations comes out to be$f_o = 16\ (N/\ 2^n)$ kHz.

In this researchwork, the digital control word(N) is 4-bit long (i.e., n=4). From the previous expression, the frequency of oscillations for N=1 comes out to be 1 kHz. Table (1) shows the other results of frequency of oscillations for N=4, 9, & 16. Theoutputs of digitally tuned quadrature oscillator obtained are shown in figures (8-11). Figure (12) illustratesthat the experimental value of frequency of oscillations closely overlapsthe theoretical value for which the oscillator was designed and linearly varies with digital control word (N).Due to the unpredictability in the value of the gate to source voltage of NMOS transistors (used for switching purpose), the results deviate from the theoretical one.

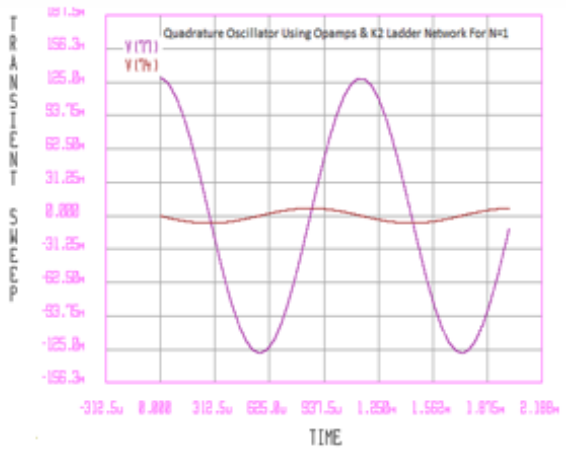


Fig. (8) Output Waveforms of Quadrature Oscillator for Control Word N=1

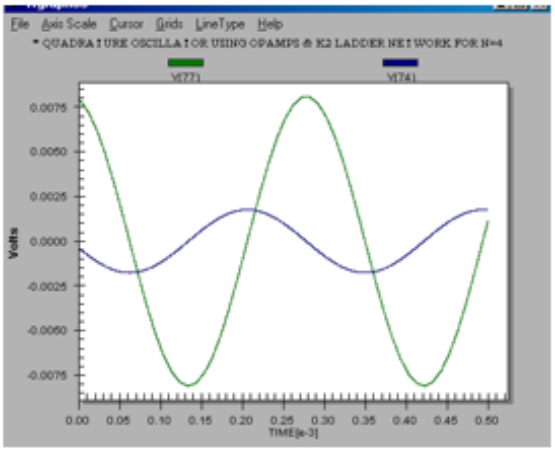


Fig. (9) Output Waveforms of Quadrature Oscillator for Control Word N=4

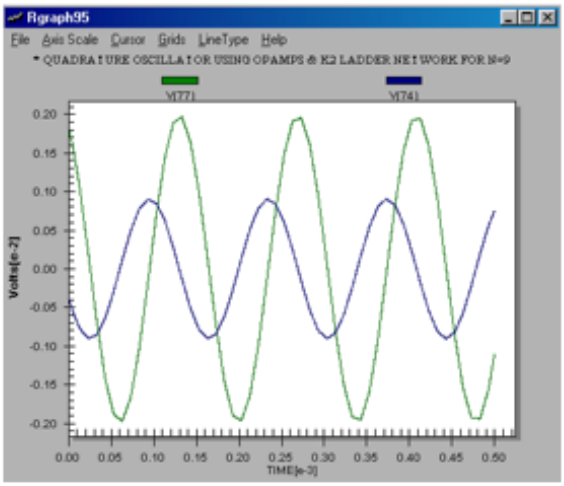


Fig. (10) Output Waveforms of Quadrature Oscillator for Control Word N=9

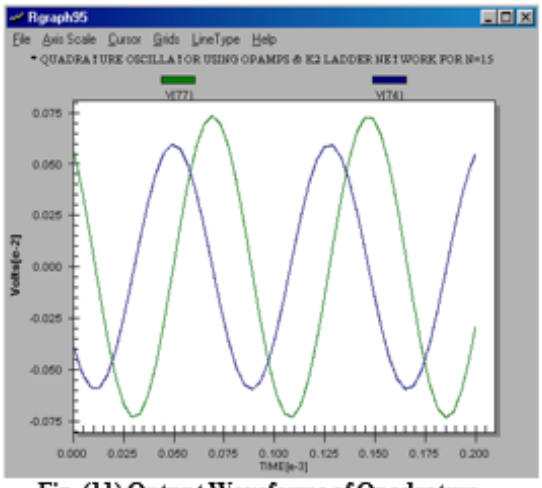


Fig. (11) Output Waveforms of Quadrature Oscillator for Control Word N=15

Table (1) Theoretical & Practical Frequency of Oscillations for various Digital Control Words

S. No.	Digital Control Word (N)	Frequency of Oscillations	
		Theoretical Value (kHz)	Practical Value (kHz)
1.	1	1	0.84
2.	4	4	3.57
3.	9	9	8.33
4.	15	15	14.29

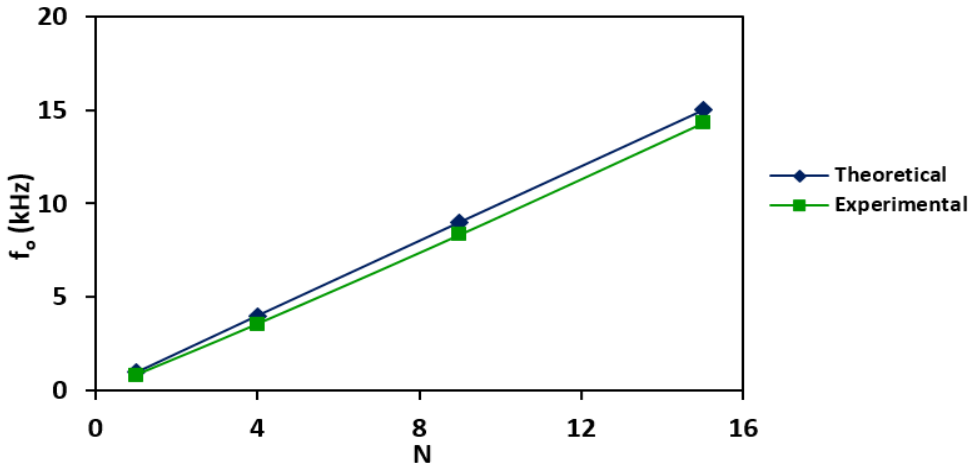


Fig. (12) Graph between Frequency of Oscillations versus Digital Control Word (N)

V.CONCLUSION

The results in the plots show the simulated outputs in PSPICE, which are in conformity with the theory. The simulation of this oscillator has been verified using only 4-bit ladder circuit. However, for a still higher range of frequency tuning, the number of bits may be increased. Of course, the higher range of frequency tuning is feasible at an additional cost of hardware because with every bit, an additional R-2R elements are added to the main ladder circuit.From the study and design of the digitally tuned oscillator, it has been analysed that the frequency of oscillations for which quadrature oscillator circuit was designed deviates slightly from the theoretical value which is due to the unpredictability of terminal voltages (i.e. gate to source voltages) of the MOSFETs whose ON-resistance has been used. This variation in terminal voltages causes the variation of ON-resistance of the transistors, which is included with the 2R-resistor in the ladder network circuit. But for best results the ratio of both resistances 2R and R must be exactly 2. The solution to this problem is to use the NMOS transistors as switches whose ON-resistance is independent of terminal voltages. The care must also be taken into account that the value of resistance R connected at the output of a buffer circuitin the digitally tuned quadrature oscillator circuit should be very high as compared to the output resistance of the Op-Amp (i.e., 75Ω) to avoid loading effect.

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