

DESIGN AND SIMULATION OF DIGITALLY PROGRAMMABLE ANALOG FILTERS

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ABSTRACT

This research work is the implementation of digitally programmable continuous time first and second order filter sections (Low pass, High pass, and Band pass). Digitally programmable devices are very useful in today's world because now the trend is of designing the hybrid systems (due to the advances in IC technology), to benefit the advantages of both the analog and digital world and these digitally programmable filters (DPFs) will be convenient from the point of view of interfacing. A digital control word (n-bit long) controls the wide adjustment range of the 3- dB frequencies of filter structures. The software implementation of the filters has been done using PSPICE on Windows platform. Because of small size/high density and low power consumption of MOSFETS on the IC chip, these transistors have been used for switching purpose in this research work to reduce area and operating voltage.

Keywords: OTA, R-2R Ladder Circuit; Analog Switch Array; Digitally Programmable Resistor; Digitally Programmable Inductor; Electronically Tuned Filters.

I. INTRODUCTION

Continuous time signal processing (e.g., signal filtering) is required in many signal processing applications and continuous time approach is capable to operate at high frequencies than the sampled data counterpart such as switched capacitor and digital filtering approaches. Filters based on Op-Amp are restricted in their applications because of the frequency dependent gain and non-availability of active RC analog filters in monolithic form. Therefore, to combat these shortcomings a more natural gain device, OTA (operational transconductance amplifier) is used, which is basically a differential voltage controlled current source (DVCCS). It has an extra control of its transconductance g_m with the help of its bias current, I_b over several decades. In general, the OTA based circuits offer advantages of simplicity in design, lower component count, reliable high frequency operation, and wide range tunability over Op-Amp based circuits. Op-Amp based active-RC filters are highly linear but limited bandwidth and lack of programmability restricts their use in discrete world. The advancement in IC technology has led the recent trend of designing hybrid systems, to benefit the advantages of both the analog and discrete world. This requires control of analog and discrete world through digital means in modern communication, electronic instrumentation and control systems. The adjusting continuous time structures data programmable over a wide range also suffer from significant dynamic RAM degradation with the adjustable parameter and fully reconfigurable continuous time structures are essentially non-existent. In this research work, digitally programmable continuous time filter structures are introduced which provide wide adjustment range, fine adjustability, and complete reconfigurability. A technique is given to provide the digital control to pursue components like resistor, capacitor, and inductor. These digitally controlled RLC elements have been employed in the realization of

analog time filters, which in turn can also be controlled digitally. Also some digitally controlled building blocks have been introduced in the universal biquadratic filters, which provide digital programmability to continuous time filters. As far as this work is concerned, a scheme has been developed for digital control of continuous time (analog) systems [1-3].

II. ELECTRONICALLY TUNED FILTERS

The characteristic features of a filter are its gain, bandwidth, and centre frequency (for BPF). In certain applications, it is desirable to vary these parameters. This is referred to as tuning or programming of filters. Tunable filters are an important constituent of radio receivers in which the RF section has one or more such filters for the purpose of receiving signals over a wide range of frequencies. Spectrum analysers also make use of tuned filters to allow only the desired frequency components. The tuning process is either manual or electronic. The familiar transistor has tuning knob, which is rotated by a user to catch or, tuned to a particular station. Similarly, in signal generators a particular frequency is selected by manual tuning. Electronic tuning achieves the same purpose by suitable electrical signals. The tuning may be either through voltage or current [4].

2.1 VOLTAGE TUNING

The varactor diode is an excellent example of voltage tuned device. When a diode is reverse biased, a depletion region is created which contains uncovered immobile charges. The thickness of the space charge region increases with reverse voltage. This may be considered as capacitive effect and the associated capacitance is termed as transition capacitance. For a step-graded junction, it varies as square root of junction voltage and for the linearly graded junction, the variation is as cube root. A varactor diode is specially made for tuning. A field effect transistor can be used as a voltage variable resistor (VVR). The VVR effect is seen only in the region before pinch off. The controlling voltage is the gate to source voltage and the range of resistance variation is small [5].

2.2 CURRENT TUNING

The OTA is best suitable for current tuned systems. The transconductance (g_m) of the OTA is a function of the bias current (I_b) and this bias current can be used for programming the filter. It means that it is possible to tune the filter by controlling the current. The symbolic representation and equivalent circuits of OTA are shown in figure (1). The transconductance gain is proportional to the bias current. The proportionality constant (k) is dependent on temperature and device geometry. The relationship is given below:

$$g_m = k I_b = \frac{I_b}{2V_T} \quad (1)$$

where, V_T is thermal equivalent voltage (26 mV at 300 °K)

The output current, I_o of the OTA is given by:

$$I_o = g_m (V^+ - V^-) \quad (2)$$

From above two equations, we can observe that the OTA based circuits are considered programmable as the bias current may be varied using biasing circuit. The important practical limitation of OTA is the limited range of the input signal ($\leq 20\text{mV}$) that must be obeyed if the linear operation is required [6-7].

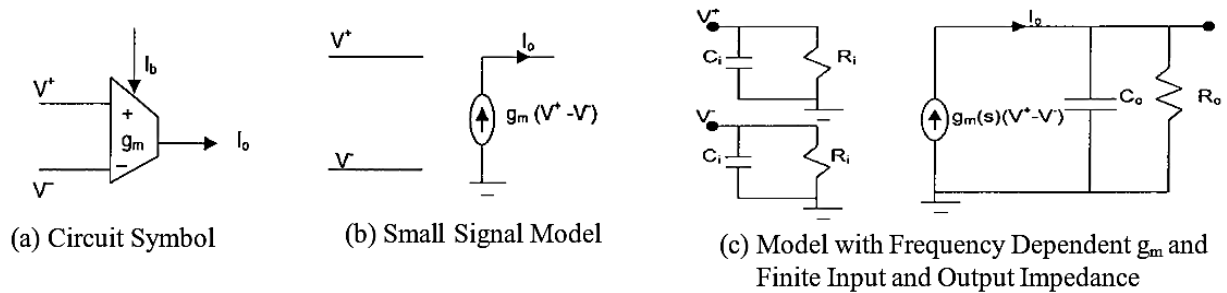


Fig. (1) Operational Transconductance Amplifier (OTA)

1.2.3 DIGITAL PROGRAMMABLE TUNING

The digitally programmable filters are widely used in computer controlled systems, e.g., frequency-synthesis, instrumentation, & data-transmission etc. In this research work, digitally controlled resistor, inductor and R-2R ladder networks (1-stage & 2-stage) have been used to implement the digitally programmable analog filters. An n-bit digital input word (N) controls the resistance or inductance, which in turn determines the cut-off frequency. The advantage of this approach is the possibility of interfacing the analog filters to the digital circuits for a better control [8-10].

III. DESIGNING OF PROGRAMMABLE ANALOG FILTERS

Programmable, as the name indicates, involves the variation of some important parameter of a device, e.g., the values of resistor, inductor, & capacitor and the 3-dB frequency of a filter in some specified manner. For example, the parameter may be changed in a continuous way or digitally (step change). Both the approaches have their own merits and demerits. In this work, the second approach is adopted in which the parameter value changes by an integral multiple of a fundamental value [11-12]. The different sub-circuits used in the design and simulation of digitally programmable analog filter circuits are discussed below:

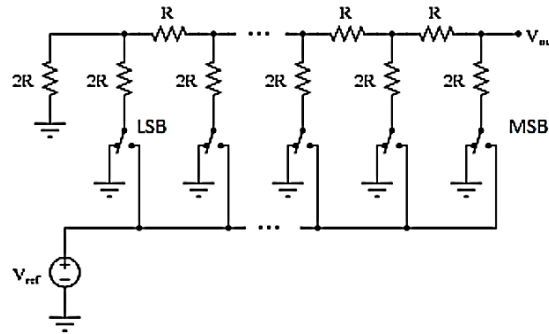
3.1 DIGITAL CONTROLLER USING R-2R LADDER NETWORK

In order to perform digital to analog conversion, R-2R ladder network as shown in figure (2) is used and the value in digital code can be converted to its corresponding voltage or current using equation (3). The converted value is also discrete in nature but when the step size is small (i.e., the number of control bits is large) it can be considered approximately as an analog quantity. The binary data inputs ($D_0, D_1, \dots, D_{n-1}$) are taken from the output register array of a digital system. The value of output voltage or current is determined by n-bits namely, $D_0, D_1, \dots, D_{n-1}$ and the reference voltage (V_{ref}). The output voltage for the circuit given in figure (2) is given by the following relationship [13-14]:

$$V_o = (2^0 D_0 + 2^1 D_1 + 2^2 D_2 + \dots + 2^{n-1} D_{n-1}) V_{ref} / 2^n$$

$$\Rightarrow V_o = (N / 2^n) V_{ref} \quad (3)$$

where, $N = (2^0 D_0 + 2^1 D_1 + 2^2 D_2 + \dots + 2^{n-1} D_{n-1})$ is the digital control word.



(2) Digital to Analog Converter (DAC) using R-2R Ladder Network

3.21/2-STAGE R-2R LADDER NETWORKS

In R-2R ladder circuit, the output is proportional to the control word. In this research work, K_1 is representing the transfer function (i.e., $K_1 = V_o / V_{ref}$) of 1-stage R-2R ladder network as shown in block diagram of figure (3a) whose value can be derived from equation (3) which can be written as:

$$K_1 = \frac{N}{2^n} \quad (4)$$

and, the output of 1-stage R-2R ladder circuit is defined as:

$$V_o = K_1 V_{ref} \quad (5)$$

The 2-stage R-2R ladder network block consists of two 1-stage R-2R ladder networks in cascade connected through a buffer circuit (a unity gain amplifier). The same control word (N) is fed to both K_1 -blocks. The 2-stage R-2R ladder network is represented by K_2 and its block diagram is illustrated in figure (3b). The output of the two stage ladder circuit is given by:

$$V_o = K_1 \cdot K_1 V_{ref} \quad (6)$$

or, $V_o = K_2 V_{ref}$

where, $K_2 = K_1 \cdot K_1 = (N/2^n)^2$

$$\Rightarrow K_2 = (N/2^n)^2 \quad (7)$$

Therefore, the transfer function of this ladder circuit is simply K_2 .

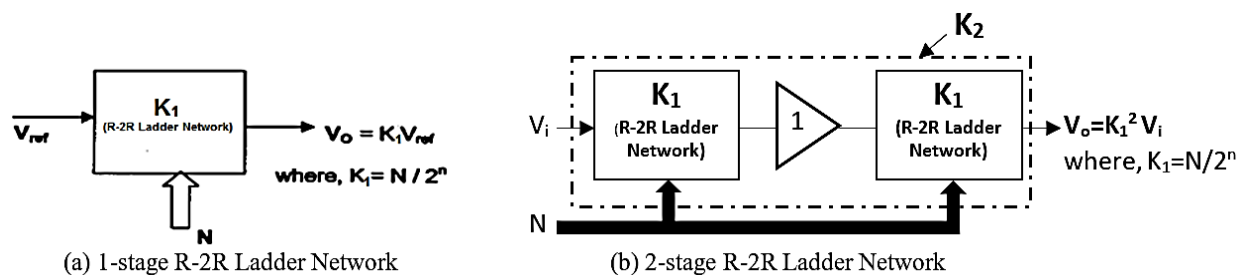


Fig. (3) Block Diagrams of R-2R Ladder Networks

3.3 R-2R LADDER NETWORK DRIVEN BY DIGITAL CONTROL WORD

A digital system (i.e., the outputs of a register array) generates the digital control word (N) that is fed to the analog switch array which in turn controls the signal levels of the inputs to R-2R ladder network. In this particular work, an analog switch array (consisting of NMOS transistors and CMOS inverters) is being used as an interface between R-2R ladder network and digital control word as shown in figure (4). Here, R-2R ladder network has been specifically designed for 4-bits only but this can be extended also for n-bits by simply adding

the R-2R resistance in parallel. The analog switch array connects resistors 2R conditionally either to the reference input voltage (V_{ref}) or ground in accordance with the bits in the digital control word, N. If the particular bit is high, the resistor is connected to V_{ref} while it is connected to ground when the bit is low because one transistor is ON and the other is OFF. A number of transistors may be used as switching device but NMOS transistors are more suitable here since they have constant ON-resistance in the ohmic region. In this research work, the ON-resistance of NMOS transistor is being added with 2R resistance in both the cases (whether the control bit is 0 or 1). In order to operate the transistor in the ohmic region, the gate to source voltage must be greater than the threshold voltage of the NMOS transistor and as far as the ladder circuit is concerned, the ratio of the resistors must remain constant that is 2. As the value of V_{ds} is assumed to be very small as compared to V_{gs} , thus, the ON-resistance of the NMOS can be defined as [15]:

$$R_{ON} = \frac{L}{W K'_N (V_{gs} - V_t)}; (V_{gs} - V_t) > 0, V_{ds} < (V_{gs} - V_t) \quad (8)$$

where, L is the channel length, W is the channel width and $K'_N = 2.5 \times 10^{-5} \text{ A/V}^2$ is transconductance. In this particular work, the values of L and W are chosen such that the R_{ON} is of $1\text{k}\Omega$ and W/L ratio from equation (8) comes out to be 10 when $V_{gs} = 5\text{V}$ and $V_t = 1\text{V}$.

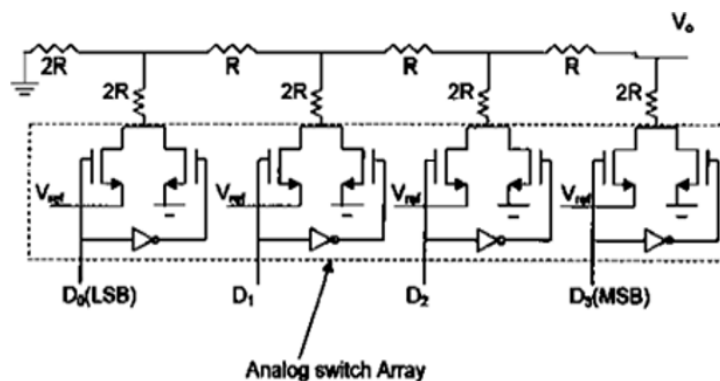


Fig. (4) R-2R Ladder Network driven by Digital Control Word

3.4 DIGITALLY PROGRAMMABLE RESISTOR

The higher values of resistor requires a lot of area on the integrated chip, therefore, active devices (like OTA) in IC-form simulate the resistors. If the output of the OTA is connected with the inverting terminal and non-inverting terminal is grounded, then the input impedance of the circuit is equivalent to a grounded resistor as shown in figure (5) and the equivalent resistance of a digitally programmable resistor is given by:

$$R_{eq} = 1/(g_m K_1) \\ \Rightarrow R_{eq} = \frac{2^n}{g_m N} \quad (9)$$

Thus, the value of resistance can be varied by varying the value of the digital control word (N).

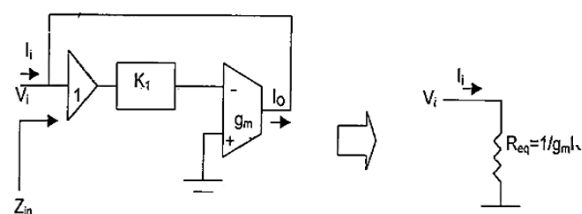


Fig. (5) Digitally Programmable Grounded Resistor

3.5 DIGITALLY PROGRAMMABLE INDUCTOR

The use of inductor in the passive circuits creates a lot of problems. At audio frequencies, high quality inductors tend to become bulky and expensive. The fabrication of inductor on integrated chip is practically not feasible. Therefore, there is a need to realize the inductor using active components. Due to inherent advantages of OTAs, it is possible to realize a grounded inductor as shown in figure (6) and the equivalent inductance of a digitally programmable inductor is given by:

$$L_{eq} = C_1 / (g_{m1} g_{m2} K_2)$$

$$\Rightarrow L_{eq} = \frac{C_1}{g_{m1} g_{m2} (N/2^n)^2} \quad (10)$$

Thus, the digital control word (N) controls the value of simulated inductor, L_{eq} .

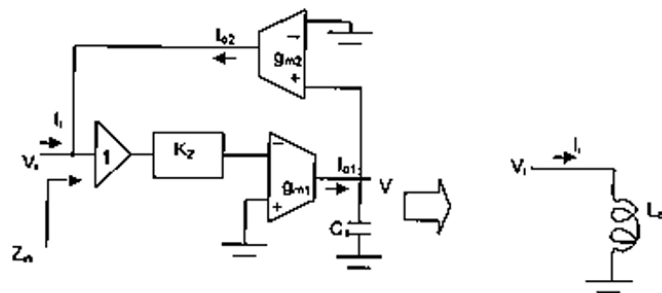


Fig. (6) Digitally Programmable Grounded Inductor

IV. SIMULATION OF DIGITALLY PROGRAMMABLE FILTERS (DPFs)

A filter is a network used to shape the frequency spectrum of an electrical signal. It is an integral component of communication and control systems. The filtering process separates an information bearing signal from undesirable interference, noise and distortion. All the filters are characterized by their frequency response, which is generally a plot of gain versus frequency of input signal.

4.1 LOW PASS FILTER

The realization of digitally programmable lowpass filter of first order is shown in figure (7), where K_1 in conjunction with buffer is connected to non-inverting terminal of OTA. The analysis of the circuit is very simple that is given below:

$$V_o = I_o / sC \text{ and } I_o = g_m (V_i - K_1 V_o)$$

$$\Rightarrow V_o (sC + g_m K_1) = g_m V_i$$

Hence, the transfer function is given by:

$$H(s) = \frac{g_m / C}{s + g_m K_1 / C} \quad (11)$$

The expression given by equation (11) shows that the cut-off frequency is a function of the transconductance (g_m) which in turn depends on the bias current. Hence, the filter can be tuned by controlling this current. Now, the cut-off frequency is given as:

$$f_o = \frac{g_m K_1}{2\pi C}$$

$$\text{or, } f_o = \frac{g_m}{2\pi C} \cdot \frac{N}{2^n} \quad (12)$$

Thus, the cut-off frequency of the digitally programmable low pass filter is digitally variable with digital control word.

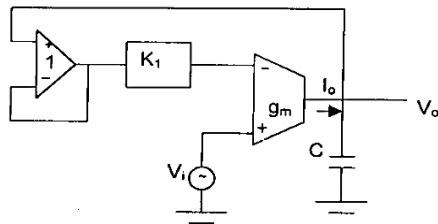


Fig. (7) Circuit Diagram of First Order Digitally Programmable Low Pass Filter

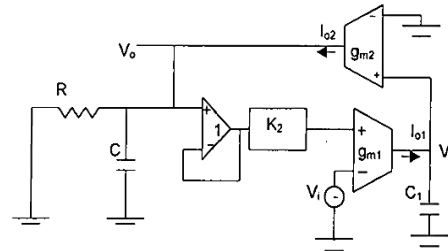


Fig. (8) Circuit Diagram of Second Order Digitally Programmable Low Pass Filter

The second order low-pass filter circuit is shown in figure (8) which is digitally programmable and the transfer function is given by the following expression:

$$H(s) = \frac{g_{m1}g_{m2}K_2/CC_1}{s^2 + s/RC + g_{m1}g_{m2}K_2/CC_1} \quad (13)$$

The standard transfer function of the second order low-pass filter is given as:

$$H_{LP}(s) = \frac{K'w_o^2}{s^2 + (w_o/Q)s + w_o^2} \quad (14)$$

By comparing equations (13) & (14), the following constants are derived here:

Gain constant, $K' = 1$

Cut-off Frequency, $f_o = 1/2\pi(g_{m1}g_{m2}K_2/CC_1)^{1/2}$

Bandwidth, $B = 1/2\pi CR$

Quality factor, $Q = R(g_{m1}g_{m2}CK_2/C_1)^{1/2}$

Assuming that the OTAs are matched, i.e., $g_{m1} = g_{m2} = g_m$ & $C_1 = C$ and substituting the value of K_2 in the above expressions, we have:

$$f_o = \frac{g_m}{2\pi C} \cdot \frac{N}{2^n} \quad \text{and} \quad Q = g_m R \cdot \frac{N}{2^n}$$

The above two expressions show that both the cut-off frequency as well as quality factor of a digitally programmable second order low pass filter are directly proportional to digital control word (N).

4.2 HIGH PASS FILTER

The transfer function of the first order high pass filter circuit of figure (9) is given as:

$$H(s) = \frac{s}{s + 1/RC} \quad (15)$$

The standard transfer function of a first order high pass filter is defined as:

$$H_{HP}(s) = \frac{K's}{s + w_o} \quad (16)$$

After comparing equations (15) & (16), the following parameters are obtained as:

Gain constant, $K' = 1$

Cut-off frequency, $w_o = 1/RC$, $f_o = 1/2\pi RC$

The cut-off frequency (f_o) depends on resistor and capacitor. Thus, the programmability can be achieved by making

any of these components variable. In this work, the grounded resistor is replaced by its digitally programmable

counterpart and the final circuit is shown in figure (9).

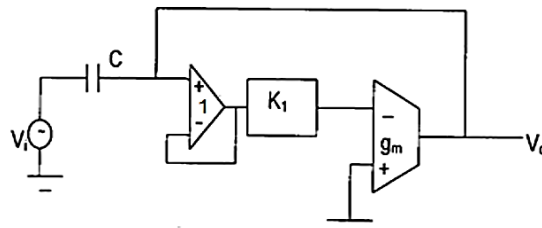


Fig. (9) Circuit Diagram of First Order Digitally Programmable High Pass Filter

Now, the cut-off frequency after replacing resistance is given as:

$$f_o = (1/2\pi g_m C)(N/2^n)$$

The above expression shows that the cut-off frequency of the digitally programmable high pass filter is directly proportional to digital control word (N).

4.3 BAND PASS FILTER

The transfer function of a second order band pass filter circuit of figure (10) is given by the following expression:

$$H(s) = \frac{s/RC}{s + s/RC + 1/LC} \quad (17)$$

The standard transfer function of a second order band pass filter is given as:

$$H_{BP}(s) = \frac{K'(w_o/Q)s}{s^2 + (w_o/Q)s + w_o^2} \quad (18)$$

After comparing equations (17) & (18), the following constants are obtained:

Gain constant, $K' = 1$

Centre frequency, $f_o = 1/2\pi(LC)^{1/2}$

Bandwidth, $B = 1/2\pi CR$

Quality factor, $Q = R(C/L)^{1/2}$

From the above relations, it is found that the aforesaid filter parameters depend on C, L, and R, therefore, the programmability can be achieved by making anyone of these components programmable. Since, the centre frequency depends on inductance as well as capacitance and either of them could be used to vary the centre frequency. In this work, the grounded inductor is replaced by its digitally programmable counterpart and the complete circuit is shown in figure (10).

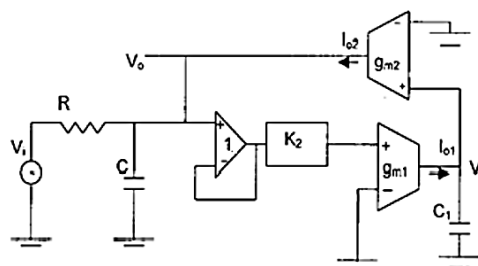


Fig. (10) Circuit Diagram of Second Order Digitally Programmable Band Pass Filter

Now, the cut-off frequency after replacing inductance is given as:

$$f_o = \frac{1}{2\pi} \left[\frac{g_{m1}g_{m2}}{CC_1} \right]^{1/2} \frac{N}{2^n}$$

Assuming the OTAs are matched, i.e., $g_{m1} = g_{m2} = g_m$ and $C_1 = C$, then f_o becomes:

$$f_o = \frac{g_m N}{2\pi C 2^n}$$

Finally, above expression shows that the centre frequency of the digitally programmable band pass filter is directly proportional to digital control word (N).

V. SIMULATION RESULTS & DISCUSSION

The development of the digitally programmable filters has been discussed step by step and the theoretical analysis has revealed that the cut-off frequency shows the expected variation as the digital control input, N is changed. The values of the voltages assumed at different terminals of NMOS transistors used for switching purposes never exist. Therefore, all filter circuits are simulated using PSPICE simulation tool [16] to verify the predicted outputs. The output voltage versus frequency curves having different values of digital control word (N: 4-bits) for different digitally programmable filters are shown in figures (11-22) and the variation of cut-off frequency (f_o) with digital control word (N) has been shown in the figures (23-25). As per table (1) and its corresponding curves for different filters (LPF, HPF, & BPF), the cut-off frequencies are very close to the theoretical values as calculated in the following sections (1.5.1-1.5.3) for which they were designed. The practical values of the cut-off frequency have slight deviation from the theoretical one and this deviation is due to the unpredictability of gate to source voltage of the NMOS transistors used for switching purposes.

5.1 For Low Pass Filter

The cut-off frequency is given by:

$$f_o = 48(N/2^n) \text{ kHz, for } C = 63 \text{ pF \& } g_m = 1.9 \times 10^{-5} \text{ S}$$

Therefore, the cut-off frequency for $N = 1$ and $n = 4$ comes out to be $f_o = 3 \text{ kHz}$. Table (1) shows other values of f_o for $N = 4, 9, 15$. Figures (11) to (14) show the results for $N (1, 4, 9, \& 15)$ respectively. The practical values are very near to the theoretical values.

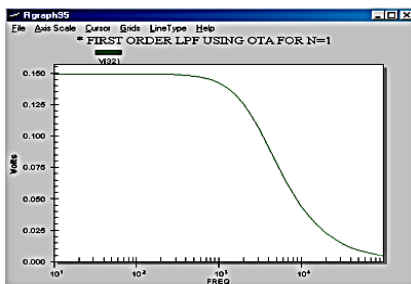


Fig. (11) Frequency versus Voltage Curve of First Order Low Pass Filter for Control Word N=1

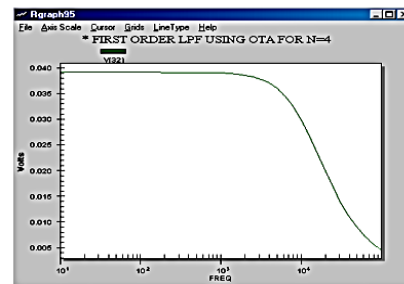


Fig. (12) Frequency versus Voltage Curve of First Order Low Pass Filter for Control Word N=4

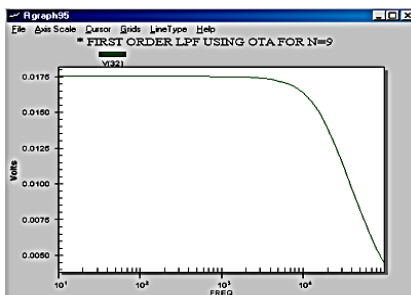


Fig. (13) Frequency versus Voltage Curve of First Order Low Pass Filter for Control Word N=9

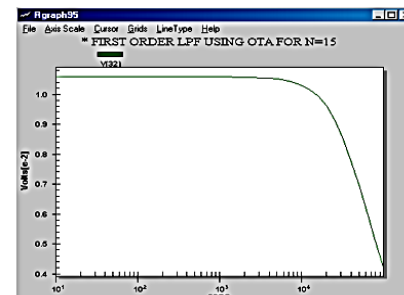


Fig. (14) Frequency versus Voltage Curve of First Order Low Pass Filter for Control Word N=15

5.2 For High Pass Filter

The cut-off frequency is given by:

$$f_o = 302.4 (N/2^n) \text{ Hz, for } C = 10 \text{ nF \& } g_m = 1.9 \times 10^{-5} \text{ S}$$

Therefore, the cut-off frequency for $N = 1$ and $n = 4$ comes out to be $f_o = 18.9 \text{ Hz}$. Table (1) shows other values of f_o for $N=4, 9, 15$. Figures (15) to (18) show the results for N (1, 4, 9, & 15) respectively. The practical values almost match with the theoretical values.

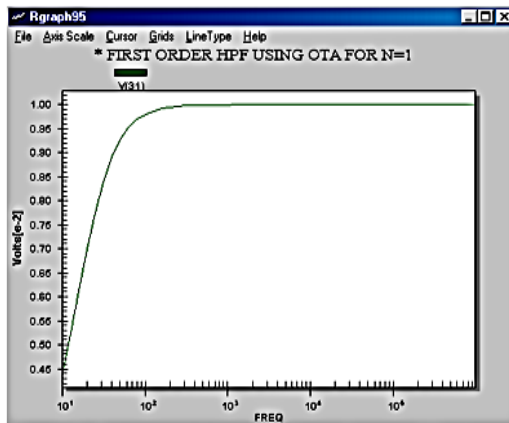


Fig. (15) Frequency versus Voltage Curve of First Order High Pass Filter for Control Word N=1

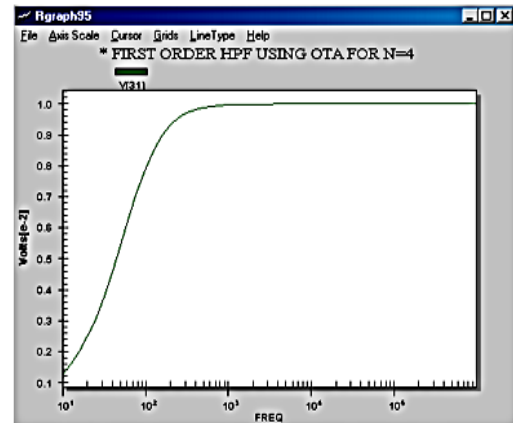


Fig. (16) Frequency versus Voltage Curve of First Order High Pass Filter for Control Word N=4

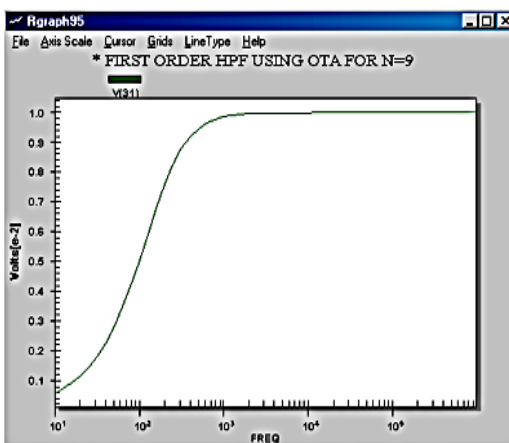


Fig. (17) Frequency versus Voltage Curve of First Order High Pass Filter for Control Word N=9

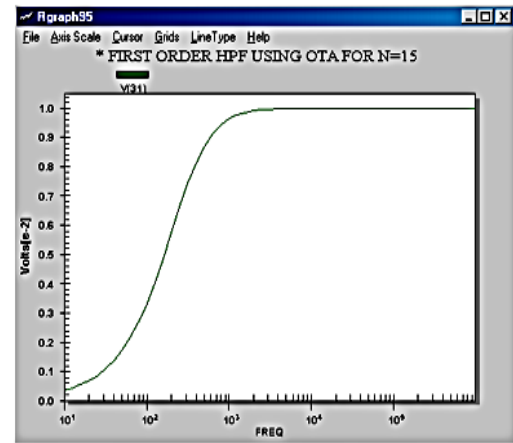


Fig. (18) Frequency versus Voltage Curve of First Order High Pass Filter for Control Word N=15

5.3 For Band Pass Filter

The centre frequency is given by:

$$f_o = 30.239 (N/2^n) \text{ kHz, for } C = C_1 = 0.1 \text{ nF \& } g_m = 1.9 \times 10^{-5} \text{ S}$$

Therefore, the centre frequency for $N = 1$ and $n = 4$ comes out to be $f_o = 1.89 \text{ kHz}$. Table (1) shows other values of f_o for $N=4, 9, 15$. Figures (19) to (22) show the results for N (1, 4, 9, & 15) respectively. The practical values almost match with the theoretical values.

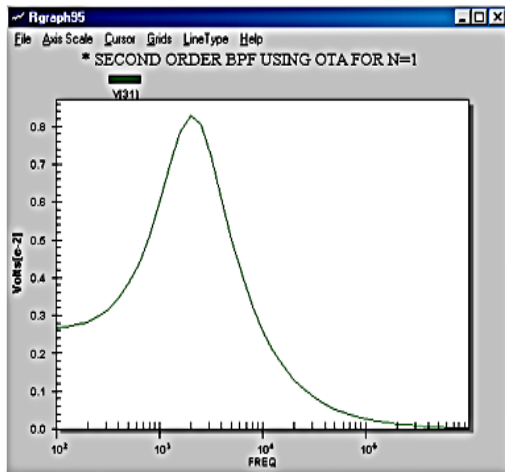


Fig. (19) Frequency versus Voltage Curve of Second Order Band Pass Filter for Control Word N=1

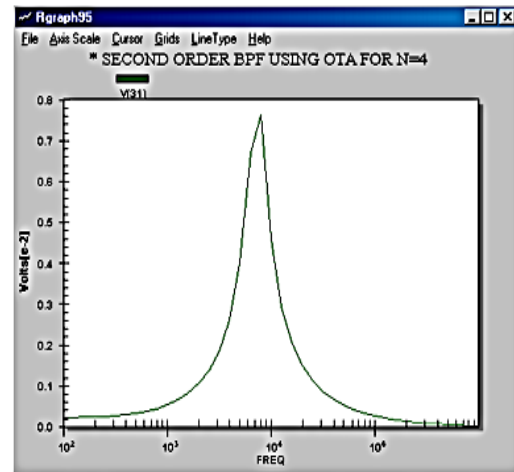


Fig. (20) Frequency versus Voltage Curve of Second Order Band Pass Filter for Control Word N=4

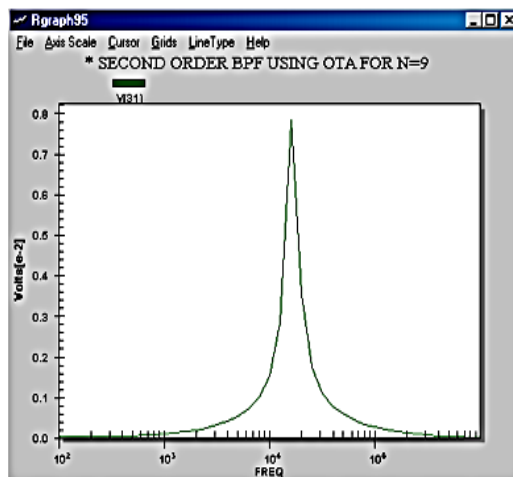


Fig. (21) Frequency versus Voltage Curve of Second Order Band Pass Filter for Control Word N=9

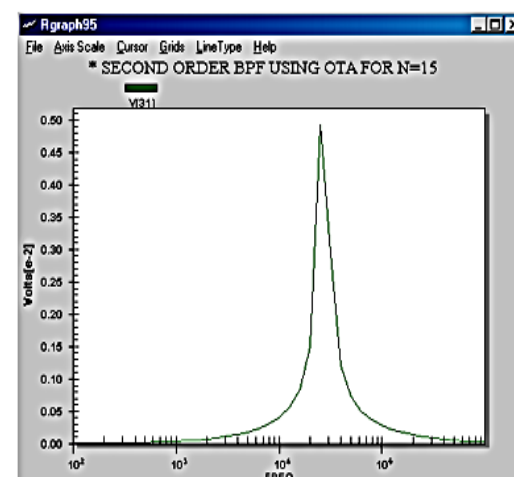


Fig. (22) Frequency versus Voltage Curve of Second Order Band Pass Filter for Control Word N=15

Table (1) Theoretical & Practical Cut-off Frequency of DPFs for varying values of N

S. No.	Digital Control Word (N)	Low Pass Filter		High Pass Filter		Band Pass Filter	
		Theoretical Value of f_c (kHz)	Practical Value of f_c (kHz)	Theoretical Value of f_c (Hz)	Practical Value of f_c (Hz)	Theoretical Value of f_c (kHz)	Practical Value of f_c (kHz)
1.	1	3	2.9	18.9	18.5	1.89	1.8
2.	4	12	11.8	75.6	75.2	7.56	7.5
3.	9	27	26.9	170.1	170	17.01	17
4.	15	45	44.6	283.5	282	28.35	28

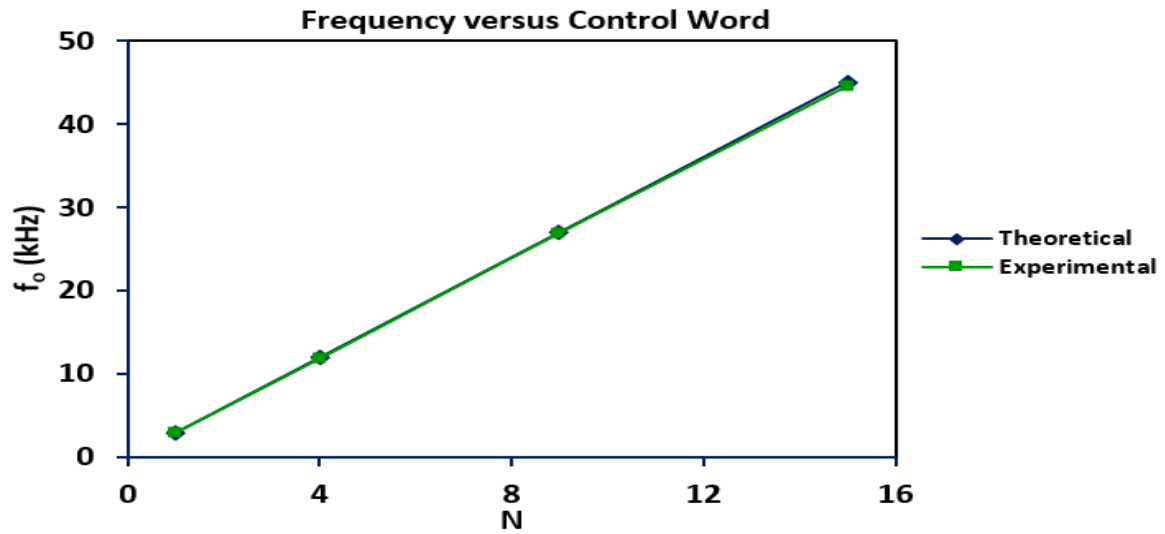


Fig. (23) Frequency versus Control Word Curve for Low Pass Filter

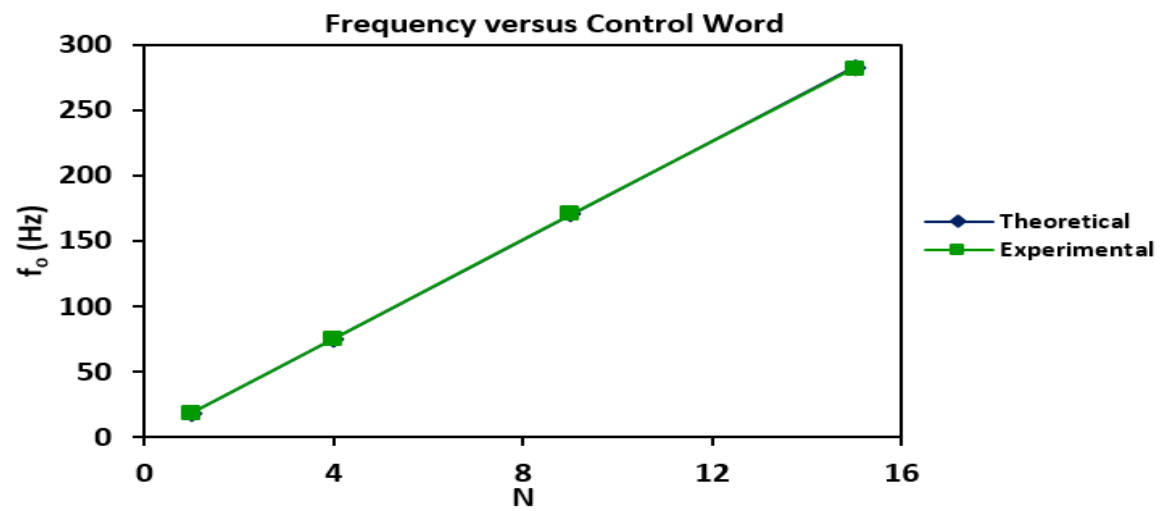


Fig. (24) Frequency versus Control Word Curve for High Pass Filter

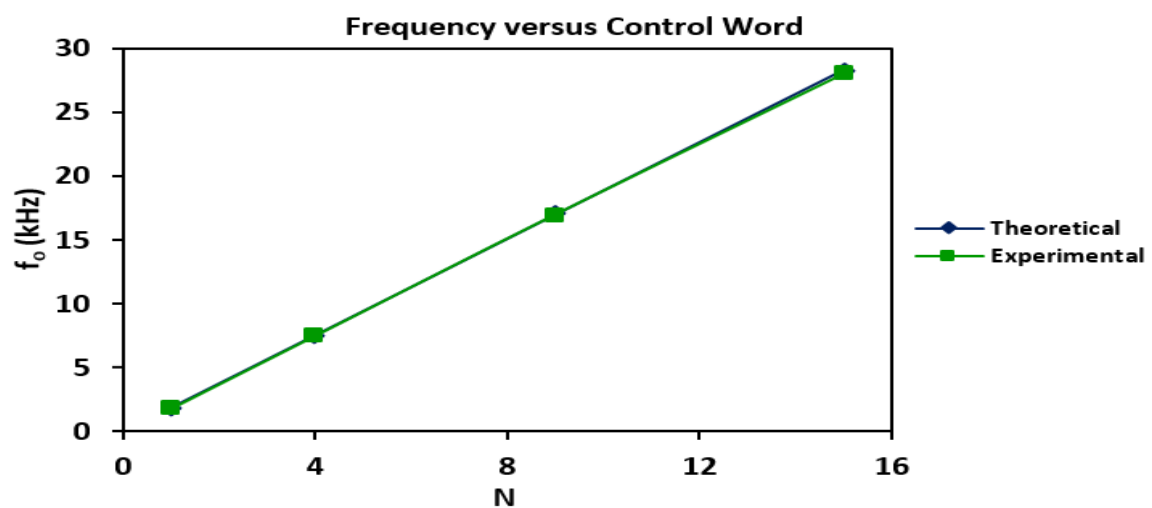


Fig. (25) Frequency versus Control Word Curve for Band Pass Filter

IV. CONCLUSION

As far as the study and design of the filter is concerned, it has been analysed that the cut-off frequency (3-dB frequency) for which the filters were designed differs slightly. The simulated outputs for various filters in PSPICE are very close to the ideal one. In order to design and simulate these filters, a 4-bit ladder circuit has been employed for getting maximum 15 cut-off frequencies (for $N=1$ to 15) but for higher range of variation of cut-off frequency and better resolution, the number of bits may be increased by just adding an additional R-2R circuit (for every new bit added) in parallel to the main ladder network which is achieved at very low cost. In this research work, the main problem with the ladder circuitry is the design of switch array using MOS transistors and of course the unpredictability of terminal voltages (i.e. gate to source voltages) of the transistors whose ON-resistance in ohmic region has been used. Due to variation in terminal voltages, the ON-resistance (which is included in the resistance, $2R$) of the transistors is varied but the ratio of both the resistances $2R$ and R must be exactly 2 in order to obtain the best results. This problem can be compensated by using NMOS switches whose ON resistance is not dependent on terminal voltages.

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