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Power Quality Improvement of Grid-Connected Dual Voltage Source Inverter system

Siva Reddy Mudiyala

Department of Electrical and Electronics Engineering,
Newton's Institute of Engineering, Macherla,(India)

ABSTRACT

This paper presents a dual voltage source inverter (DVSI) scheme to enhance the power quality and reliability of the microgrid system. The proposed scheme is comprised of two inverters, which enables the microgrid to exchange power generated by the distributed energy resources (DERs) and also to compensate the local unbalanced and nonlinear load. The control algorithms are developed based on instantaneous symmetrical component theory (ISCT) to operate DVSI in grid sharing and grid injecting modes. The proposed scheme has increased reliability, lower bandwidth requirement of the main inverter, lower cost due to reduction in filter size, and better utilization of micro- grid power while using reduced dc-link voltage rating for the main inverter. These features make the DVSI scheme a promising option for microgrid supplying sensitive loads. The topology and control algorithm are validated through extensive simulation results.

Index Terms **—Grid-Connected Inverter, Instantaneous Symmetrical Component Theory (ISCT), Microgrid, Power Quality.**

I. INTRODUCTION

Technological progress and environmental concerns drive the power system to a paradigm shift with more renewable energy sources integrated to the network by means of distributed generation (DG). These DG units with coordinated control of local generation and storage facilities form a microgrid. In a microgrid, power from different renewable energy sources such as fuel cells, photovoltaic (PV) systems, and wind energy systems are interfaced to grid and loads using power electronic converters. A grid interactive inverter plays an important role in exchanging power from the microgrid to the grid and the connected load. This microgrid inverter can either work in a grid sharing mode while supplying a part of local load or in grid injecting mode, by injecting power to the main grid.

Maintaining power quality is another important aspect which has to be addressed while the microgrid system is connected to the main grid. The proliferation of power electronics devices and electrical loads with unbalanced nonlinear currents has degraded the power quality in the power distribution network. Moreover, if there is a considerable amount of feeder impedance in the distribution systems, the propagation of these harmonic currents distorts the voltage at the point of common coupling (PCC). At the same instant, industry automation has reached to a very high level of sophistication, where plants like automobile manufacturing units, chemical factories, and semiconductor industries require clean power. For these applications, it is essential to compensate nonlinear and unbalanced load currents. Load compensation and power injection using grid interactive inverters

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in microgrid have been presented in the literature. A single inverter system with power quality enhancement and the main focus of this work is to realize dual functionalities in an inverter that would provide the active power injection from a solar PV system and also works as an active power filter, compensating unbalances and the reactive power required by other loads connected to the system.

A voltage regulation and power flow control scheme for a wind energy system (WES) is proposed. A distribution static compensator (DSTATCOM) is utilized for voltage regulation and also for active power injection. The control scheme maintains the power balance at the grid terminal during the wind variations using sliding mode control. A multifunctional power electronic converter for the DG power system is described. This scheme has the capability to inject power generated by WES and also to perform as a harmonic compensator. Most of the reported literature in this area discuss the topologies and control algorithms to provide load compensation capability in the same inverter in addition to their active power injection. When a grid-connected inverter is used for active power injection as well as for load compensation, the inverter capacity that can be utilized for achieving the second objective is decided by the available instantaneous microgrid real power. Considering the case of a grid-connected PV inverter, the available capacity of the inverter to supply the reactive power becomes less during the maximum solar insulation periods. At the same instant, the reactive power to regulate the PCC voltage is very much needed during this period. It indicates that providing multifunctional utilities in a single inverter degrades either the real power injection or the load compensation capabilities.

This paper demonstrates a dual voltage source inverter (DVSI) scheme, in which the power generated by the microgrid is injected as real power by the main voltage source inverter (MVSI) and the reactive, harmonic, and unbalanced load compensation is performed by auxiliary voltage source inverter (AVSI). This has an advantage that the rated capacity of MVSI can always be used to inject real power to the grid, if sufficient renewable power is available at the dc link. In the DVSI scheme, as total load power is supplied by two inverters, power losses across the semiconductor switches of each inverter are reduced. This increases its reliability as compared to a single inverter with multifunctional capabilities. Also, smaller size modular inverters can operate at high switching frequencies with a reduced size of interfacing inductor; the filter cost gets reduced. Moreover, as the main inverter is supplying real power, the inverter has to track the fundamental positive sequence of current. This reduces the bandwidth requirement of the main inverter. The inverters in the proposed scheme use two separate dc links. Since the auxiliary inverter is supplying zero sequence of load current, a three-phase three-leg inverter topology with a single dc storage capacitor can be used for the main inverter. This in turn reduces the dc-link voltage requirement of the main inverter. Thus, the use of two separate inverters in the proposed DVSI scheme provides increased reliability, better utilization of microgrid power, reduced dc grid voltage rating, less bandwidth requirement of the main inverter, and reduced filter size. Control algorithms are developed by instantaneous symmetrical component theory (ISCT) to operate DVSI in grid-connected mode, while considering non stiff grid voltage. The extraction of fundamental positive sequence of PCC voltage is done by *dq*0 transformation. The control strategy is tested with two parallel inverters connected to a three-phase four-wire distribution system. Effectiveness of the proposed control algorithm is validated through detailed simulation results.

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II. DUAL VOLTAGE SOURCE INVERTER

2.1 System Topology

The proposed DVSI topology is shown in Fig. 1. It consists of a neutral point clamped (NPC) inverter to realize AVSI and a three-leg inverter for MVSI .

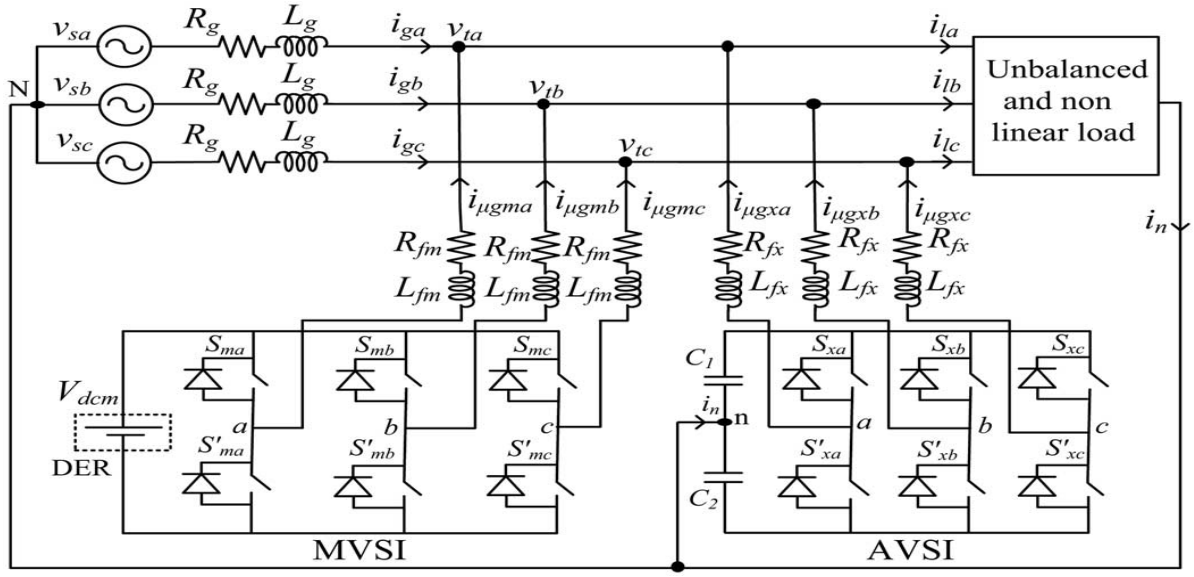

Fig.1. Topology of proposed DVSI scheme.

These are connected to grid at the PCC and supplying a nonlinear and unbalanced load. The function of the AVSI is to compensate the reactive, harmonics, and unbalance components in load currents. Here, load currents in three phases are represented by i_{la}, i_{lb}, and i_{lc}, respectively. Also, $i_{g(abc)}$, $i_{\mu gm(abc)}$, and $i_{\mu gx(abc)}$ show grid currents, MVSI currents, and AVSI currents in three phases, respectively. The dc link of the AVSI utilizes a split capacitor topology, with two capacitors C_1 and C_2. The MVSI delivers the available power at distributed energy resource (DER) to grid. The DER can be a dc source or an ac source with rectifier coupled to dc link. Usually, renewable energy sources like fuel cell and PV generate power at variable low dc volt- age, while the variable speed wind turbines generate power at variable ac voltage. Therefore, the power generated from these sources use a power conditioning stage before it is connected to the input of MVSI. In this study, DER is being represented as a dc source. An inductor filter is used to eliminate the high-frequency switching components generated due to the switching of power electronic switches in the inverters. The system considered in this study is assumed to have some amount of feeder resistance R_g and inductance L_g. Due to the presence of this feeder impedance, PCC voltage is affected with harmonics.

2.2. Design of DVSI Parameters

2.2.1 AVSI: The important parameters of AVSI like dc-link voltage (V_{dc}), dc storage capacitors (C_1 and C_2), interfacing inductance (L_{fx}), and hysteresis band ($\pm h_x$) are selected based on the design method of split capacitor DSTATCOM topology.The dc-link voltage across each capacitor is taken as 1.6 times the peak of phase voltage. The total dc-link voltage reference (V_{dcref}) is found to be 1040 V. Values of dc capacitors of AVSI are chosen based on the change in dc-link voltage during transients. Let total load rat- ing is S kVA. In the worst case, the load power may vary from minimum to maximum, i.e., from 0 to S kVA. AVSI needs to

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exchange real power during transient to maintain the load power demand. This transfer of real power during the transient will result in deviation of capacitor voltage from its reference value. Assume that the voltage controller takes *n* cycles, i.e., *nT* seconds to act, where *T* is the system time period. Hence, maximum energy exchange by AVSI during transient will be *nST* . This energy will be equal to change in the capacitor stored energy. Therefore

$$\frac{1}{2}C_1(V_{\text{dcr}}^2 - V_{\text{dc1}}^2) = nST \qquad (1)$$

where V_{dcr} and V_{dc1} are the reference dc voltage and maximum permissible dc voltage across C_1 during transient, respectively. Here, $S = 5$ kVA, $V_{\text{dcr}} = 520$ V, $V_{\text{dc1}} = 0.8 * V_{\text{dcr}}$ or $1.2 * V_{\text{dcr}}$, $n = 1$, and $T = 0.02$ s. Substituting these values in (1), the dc- link capacitance (C_1) is calculated to be 2000 μF. Same value of capacitance is selected for C_2.

The interfacing inductance is given by

$$L_{fx} = \frac{1.6\,V_m}{4\,h_x f_{\max}}. \qquad (2)$$

Assuming a maximum switching frequency (fmax) of 10 kHz and hysteresis band (hx) as 5% of load current (0.5 A), the value of L_{fx} is calculated to be 26 mH.

2.2.2. MVSI: The MVSI uses a three-leg inverter topology. Its dc-link voltage is obtained as $1.15 * \text{Vml}$, where Vml is the peak value of line voltage. This is calculated to be 648 V. Also, MVSI supplies a balanced sinusoidal current at unity power factor. So, zero sequence switching harmonics will be absent in the output current of MVSI. This reduces the filter requirement for MVSI as compared to AVSI. In this analysis, a filter inductance (Lfm) of 5 mH is used.

2.3. Advantages of the DVSI Scheme

The various advantages of the proposed DVSI scheme over a single inverter scheme with multifunctional capabilities are discussed here as follows:

2.3.1. Increased Reliability: DVSI scheme has increased reliability, due to the reduction in failure rate of components and the decrease in system down time cost . In this scheme, the total load current is shared between AVSI and MVSI and hence reduces the failure rate of inverter switches. Moreover, if one inverter fails, the other can continue its operation. This reduces the lost energy and hence the down time cost. The reduction in system down time cost improves the reliability.

2.3.2 Reduction in Filter Size: In DVSI scheme, the current supplied by each inverter is reduced and hence the current rating of individual filter inductor reduces. This reduction in current rating reduces the filter size. Also, in this scheme, hysteresis current control is used to track the inverter reference currents. As given in (2), the filter inductance is decided by the inverter switching frequency. Since the lower current rated semiconductor device can be switched at higher switching frequency, the inductance of the filter can be lowered. This decrease in inductance further reduces the filter size.

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2.3.3. Improved Flexibility: Both the inverters are fed from separate dc links which allow them to operate independently, thus increasing the flexibility of the system. For instance, if the dc link of the main inverter is disconnected from the system, the load compensation capability of the auxiliary inverter can still be utilized.

2.3.4. Better Utilization of Microgrid Power: DVSI scheme helps to utilize full capacity of MVSI to transfer the entire power generated by DG units as real power to ac bus, as there is AVSI for harmonic and reactive power compensation. This increases the active power injection capability of DGs in microgrid.

2.3.5. Reduced DC-Link Voltage Rating: Since, MVSI is not delivering zero sequence load current components, a single capacitor three-leg VSI topology can be used. Therefore, the dclink voltage rating of MVSI is reduced approximately by 38%, as compared to a single inverter system with split capacitor VSI topology.

III. CONTROL STRATEGY FOR DVSI SCHEME

3.1. Fundamental Voltage Extraction

A. Fundamental Voltage Extraction The control algorithm for reference current generation using ISCT requires balanced sinusoidal PCC voltages. Because of the presence of feeder impedance, PCC voltages are distorted. Therefore, the fundamental positive sequence components of the PCC voltages are extracted for the reference current generation.

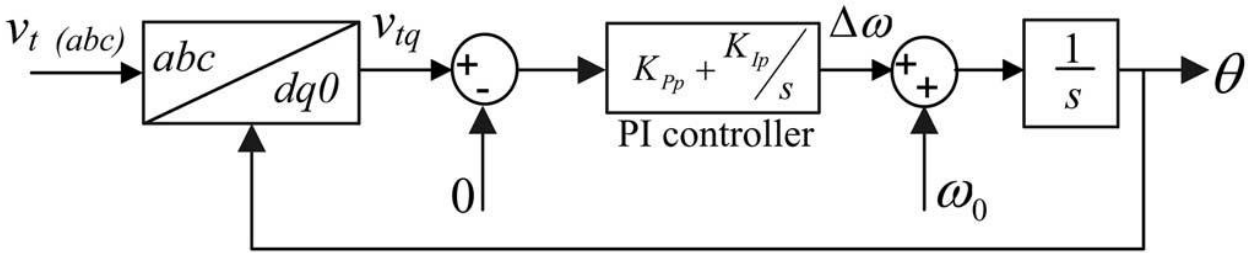

Fig. 2. Schematic diagram of PLL.

To convert the distorted PCC voltages to balanced sinusoidal voltages, dq0 transformation are used. The PCC voltages in natural reference frame (vta, vtb, and vtc) are first transformed into dq0 reference frame as given by

$$\begin{bmatrix} v_{td} \\ v_{tq} \\ v_{t0} \end{bmatrix} = C \begin{bmatrix} v_{ta} \\ v_{tb} \\ v_{tc} \end{bmatrix} \qquad (3)$$

Where

$$C = \sqrt{\frac{2}{3}} \begin{bmatrix} \sin\theta & \sin(\theta - \frac{2\pi}{3}) & \sin(\theta + \frac{2\pi}{3}) \\ \cos\theta & \cos(\theta - \frac{2\pi}{3}) & \cos(\theta + \frac{2\pi}{3}) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix}$$

In order to get θ, a modified synchronous reference frame (SRF) phase locked loop (PLL) is used. The schematic diagram of this PLL is shown in Fig. 2. It mainly consists of a proportional integral (PI) controller and an integrator. In this PLL, the SRF terminal voltage in q-axis (vtq) is compared with 0 V and the error voltage thus obtained is given to the PI controller.

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The frequency deviation Δω is then added to the reference frequency ω0 and finally given to the integrator to get θ. It can be proved that, when, θ = ω0 t and by using the Park's transformation matrix (C), q-axis voltage in dq0 frame becomes zero and hence the PLL will be locked to the reference frequency (ω0). As PCC voltages are distorted, the transformed voltages in dq0 frame (vtd and vtq) contain average and oscillating components of voltages. These can be represented as

$$v_{td} = \overline{v}_{td} + \widetilde{v}_{td}, \quad v_{tq} = \overline{v}_{tq} + \widetilde{v}_{tq} \qquad (4)$$

where vtd and vtq represent the average components of vtd and vtq, respectively. The terms vtd and vtq indicate the oscillating components of vtd and vtq, respectively. Now the fundamental positive sequence of PCC voltages in natural reference frame can be obtained with the help of inverse dq0 transformation as given by

$$\begin{bmatrix} v_{ta1}^{+} \\ v_{tb1}^{+} \\ v_{tc1}^{+} \end{bmatrix} = C^{T} \begin{bmatrix} \overline{v}_{td} \\ \overline{v}_{tq} \\ 0 \end{bmatrix}. \qquad (5)$$

These voltages *v*+*ta*1, *v*+*tb*1, and *v*+*tc*1 are used in the reference current generation algorithms, so as to draw balanced sinusoidal currents from the grid.

3.2. Instantaneous Symmetrical Component Theory

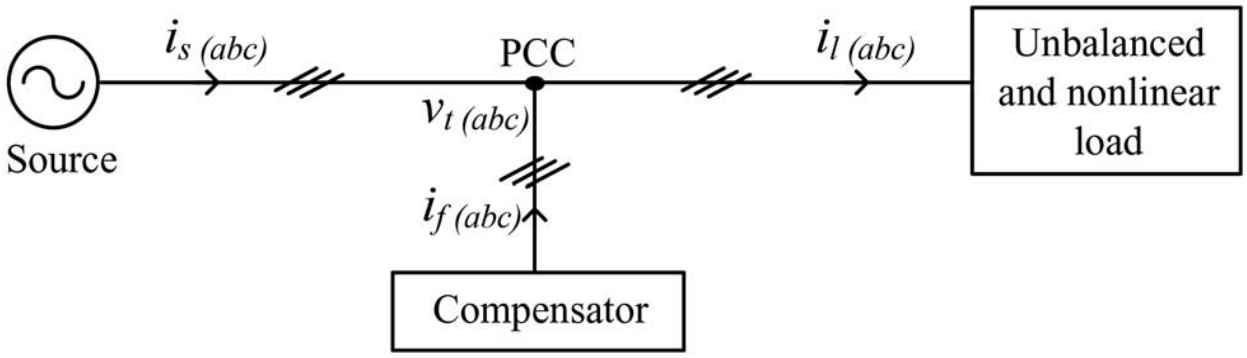

Fig. 3. Schematic of an unbalanced and nonlinear load compensation scheme

ISCT was developed primarily for unbalanced and nonlinear load compensations by active power filters. The system topology shown in Fig. 3 is used for realizing the reference current for the compensator. The ISCT for load compensation is derived based on the following three conditions.

1) The source neutral current must be zero. Therefore

$$i_{sa} + i_{sb} + i_{sc} = 0. \qquad (6)$$

2) The phase angle between the fundamental positive sequence voltage (*v*+*ta*1) and source current (*isa*) is *φ*

$$\angle v_{ta1}^{+} = \angle i_{sa} + \phi. \qquad (7)$$

3) The average real power of the load (Pl) should be supplied by the source

$$v_{ta1}^{+}\, i_{sa} + v_{tb1}^{+}\, i_{sb} + v_{tc1}^{+}\, i_{sc} = P_l. \qquad (8)$$

Solving the above three equations, the reference source currents can be obtained as

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$$i_{sa}^{*} = \left(\frac{v_{ta1}^{+} + \beta(v_{tb1}^{+} - v_{tc1}^{+})}{\sum_{j=a,b,c} v_{tj}^{+2}} \right) P_l$$
$$i_{sb}^{*} = \left(\frac{v_{tb1}^{+} + \beta(v_{tc1}^{+} - v_{ta1}^{+})}{\sum_{j=a,b,c} v_{tj}^{+2}} \right) P_l \qquad (9)$$
$$i_{sc}^{*} = \left(\frac{v_{tc1}^{+} + \beta(v_{ta1}^{+} - v_{tb1}^{+})}{\sum_{j=a,b,c} v_{tj}^{+2}} \right) P_l$$

The β= tan$\varphi/\sqrt{3}$ is the desired phase angle between the fundamental positive sequence of PCC voltage and source current. To achieve unity power factor for source current, substitute $\beta = 0$ in (9). Thus, the reference source currents for three phases are given by

$$i_{s(abc)}^{*} = \left(\frac{v_{t(abc)1}^{+}}{\sum_{j=a,b,c} v_{tj}^{+2}} \right) P_l \qquad (10)$$

where $i* sa$, $i* sb$, and $i* sc$ are fundamental positive sequence of load currents drawn from the source, when it is supplying an average load power *Pl*. The power *Pl* can be computed using a moving average filter with a window of one-cycle data points as given below

$$P_l = \frac{1}{T} \int_{t_1 - T}^{t_1} (v_{ta1}^{+} i_{la} + v_{tb1}^{+} i_{lb} + v_{tc1}^{+} i_{lc}) dt \qquad (11)$$

where *t*1 is any arbitrary time instant. Finally, the reference currents for the compensator can be generated as follows:

$$i_{f\,(abc)}^{*} = i_{l\,(abc)} - i_{s\,(abc)}^{*}. \qquad (12)$$

Equation (12) can be used to generate the reference filter currents using ISCT, when the entire load active power, *Pl* is supplied by the source and load compensation is performed by a single inverter. A modification in the control algorithm is required, when it is used for DVSI scheme. The following section discusses the formulation of control algorithm for DVSI scheme. The source currents, *is*(*abc*) and filter currents *if*(*abc*) will be equivalently represented as grid currents *ig*(*abc*) and AVSI currents *iμgx*(*abc*), respectively, in further sections.

3.3. Control Strategy of DVSI

Control strategy of DVSI is developed in such a way that grid and MVSI together share the active load power, and AVSI supplies rest of the power components demanded by the load.

3.3.1. Reference Current Generation for Auxiliary Inverter

The dc-link voltage of the AVSI should be maintained constant for proper operation of the auxiliary inverter. DC-link voltage variation occurs in auxiliary inverter due to its switching and ohmic losses. These losses termed as *P*loss should also be supplied by the grid. An expression for *P*loss is derived on the condition that average dc

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capacitor current is zero to maintain a constant capacitor voltage. The deviation of average capacitor current from zero will reflect as a change in capacitor voltage from a steady state value. A PI controller is used to generate *P*loss term as given by

$$P_{\text{loss}} = K_{Pv}\, e_{v\text{dc}} + K_{Iv} \int e_{v\text{dc}} dt \qquad (13)$$

where *ev*dc = *V*dcref − *v*dc, *v*dc represents the actual voltage sensed and updated once in a cycle. In the above equation, *KPv* and *KIv* represent the proportional and integral gains of dc-link PI controller, respectively. The *P*loss term thus obtained should be supplied by the grid, and therefore AVSI reference currents can be obtained as given in (14). Here, the dc-link voltage PI controller gains are selected so as to ensure stability and better dynamic response during load change.

$$\begin{aligned} i^*_{\mu gxa} &= i_{la} - \left(\frac{v^+_{ta1}}{\sum_{j=a,b,c} v^{+2}_{tj}}\right)(P_l + P_{\text{loss}}) \\ i^*_{\mu gxb} &= i_{lb} - \left(\frac{v^+_{tb1}}{\sum_{j=a,b,c} v^{+2}_{tj}}\right)(P_l + P_{\text{loss}}) \qquad (14) \\ i^*_{\mu gxc} &= i_{lc} - \left(\frac{v^+_{tc1}}{\sum_{j=a,b,c} v^{+2}_{tj}}\right)(P_l + P_{\text{loss}}). \end{aligned}$$

3.3.2. Reference Current Generation for Main Inverter:

The MVSI supplies balanced sinusoidal currents based on the available renewable power at DER. If MVSI losses are neglected, the power injected to grid will be equal to that available at DER (*Pμg*). The following equation, which is derived from ISCT can be used to generate MVSI reference currents for three phases (*a*, *b*, and *c*)

$$i^*_{\mu gm(abc)} = \left(\frac{v^+_{t(abc)1}}{\sum_{j=a,b,c} v^{+2}_{tj}}\right) P_{\mu g} \qquad (15)$$

where *Pμg* is the available power at the dc link of MVSI. The reference currents obtained from (14) to (15) are tracked by using hysteresis band current controller (HBCC). HBCC schemes are based on a feedback loop, usually with a two-level comparator. This controller has the advantage of peak current limiting capacity, good dynamic response, and simplicity in implementation. A hysteresis controller is a high-gain proportional controller. This controller adds certain phase lag in the operation based on the hysteresis band and will not make the system unstable. Also, the proposed DVSI scheme uses a first-order inductor filter which retains the closed-loop system stability. The entire control strategy is schematically represented in Fig. 4. Applying Kirchoff's current law (KCL) at the PCC in Fig. 4

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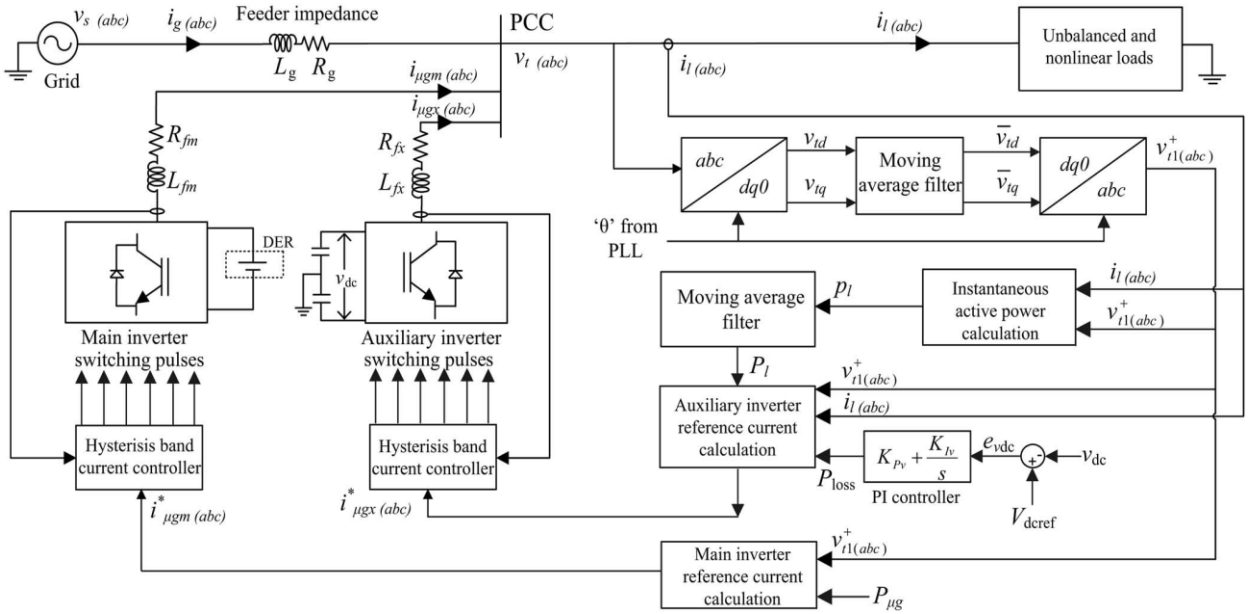

Fig. 4. Schematic diagram showing the control strategy of proposed DVSI scheme.

$$i_{\mu g x\, j} = i_{l\, j} - (i_{g\, j} + i_{\mu g m\, j}), \quad \text{for } j = a, b, c. \qquad (16)$$

By using (14) and (16), an expression for reference grid current in phase-*a* ($i*ga$) can be obtained as

$$i^*_{ga} = \left(\frac{v^+_{ta1}}{\sum_{j=a,b,c} v^{+2}_{tj}} \right) [(P_l + P_{\text{loss}}) - P_{\mu g}]\,. \qquad (17)$$

IV. SIMULATION STUDIES

The simulation model of DVSI scheme shown in Fig. 1 is developed to evaluate the performance. The simulation parameters of the system are given in Table I. The simulation study demonstrates the grid sharing and grid injecting modes of operation of DVSI scheme in steady state as well as in transient conditions.

TABLE I

SYSTEM PARAMETERS FOR SIMULATION

Parameters	Values
Grid voltage	400 V(L–L)
Fundamental frequency	50 Hz
Feeder impedance	R_g = 0.5 Ω, L_g = 1.0 mH
AVSI	$C_1 = C_2$ = 2000 μF V_{dcref} = 1040 V Interfacing inductor, L_{fx} = 20 mH Inductor resistance, R_{fx} = 0.25 Ω Hysteresis band ($\pm h_x$) = 0.1 A
MVSI	DC-link voltage, V_{dcm} = 650 V Interfacing inductor, L_{fm} = 5 mH Inductor resistance, R_{fm} = 0.25 Ω Hysteresis band ($\pm h_m$) = 0.1 A
Unbalanced linear load	Z_{la} = 35 + j19 Ω Z_{lb} = 30 + j15 Ω Z_{lc} = 23 + j12 Ω
Nonlinear load	3 ϕ diode bridge rectifier with DC side current of 3.0 A
DC voltage controller gains	K_{Pv} =10, K_{Iv} = 0.05

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The distorted PCC voltages due to the feeder impedance without DVSI scheme are shown in Fig. 5(a). If these distorted voltages are used for the reference current generation of AVSI, the current compensation will not be proper. Therefore, the fundamental positive sequence of voltages is extracted from these distorted voltages using the algorithm explained in Section III-A. These extracted voltages are given in Fig. 5(b). These voltages are further used for the generation of inverter reference currents. Fig. 6(a)–(d) represents active power demanded by load (*Pl*), active power supplied by grid (*Pg*), active power supplied by MVSI (*Pμg*), and active power supplied by AVSI (*Px*), respectively. It can be observed that, from *t* = 0.1 to 0.4 s, MVSI is generating 4 kW power and the load demand is 6 kW. Therefore, the remaining load active power (2 kW) is drawn from the grid. During this period, the sequence of PCC voltages.

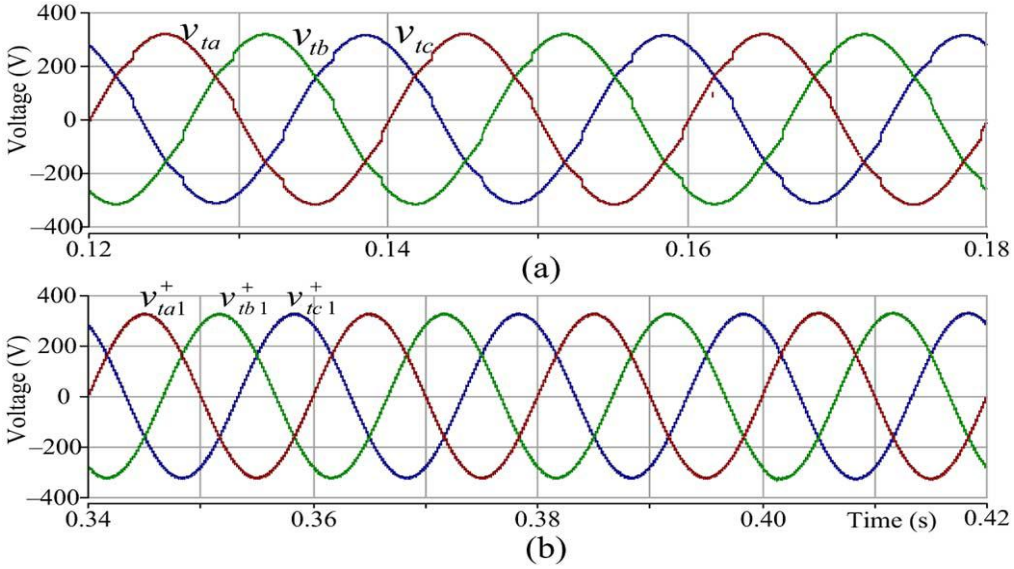

Fig. 5. Without DVSI scheme: (a) PCC voltages and (b) fundamental positive

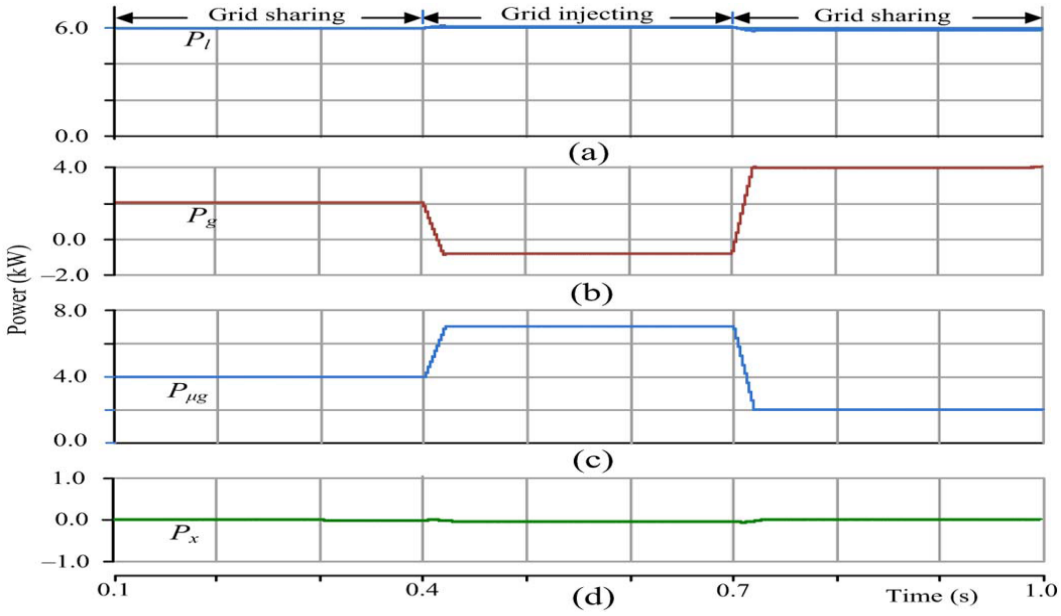

Fig. 6. Active power sharing: (a) load active power; (b) active power supplied by grid; (c) active power supplied by MVSI; and (d) active power supplied by AVSI.

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microgrid is operating in grid sharing mode. At t = 0.4 s, the microgrid power is increased to 7 kW, which is more than the load demand of 6 kW. This microgrid power change is considered to show the change of operation of MVSI from grid sharing to grid injecting mode. Now, the excess power of 1 kW is injected to the grid and hence, the power drawn from grid is shown as negative. Fig. 7(a)–(c) shows the load reactive power (Ql), reactive power supplied by AVSI (Qx), and reactive power supplied by MVSI ($Q\mu g$), respectively. It shows that total load reactive power is supplied by AVSI, as expected. Fig. 8(a)–(d) shows the plots of load currents ($il(abc)$), currents drawn from grid ($ig(abc)$), currents drawn from MVSI ($i\mu g(abc)$), and currents drawn from the AVSI ($i\mu x(abc)$), respectively. The load currents are unbalanced and distorted. The MVSI supplies balanced and sinusoidal currents during grid supporting and grid injecting modes. The currents drawn from grid are also perfectly balanced and sinusoidal, as the auxiliary inverter compensates the unbalance and harmonics

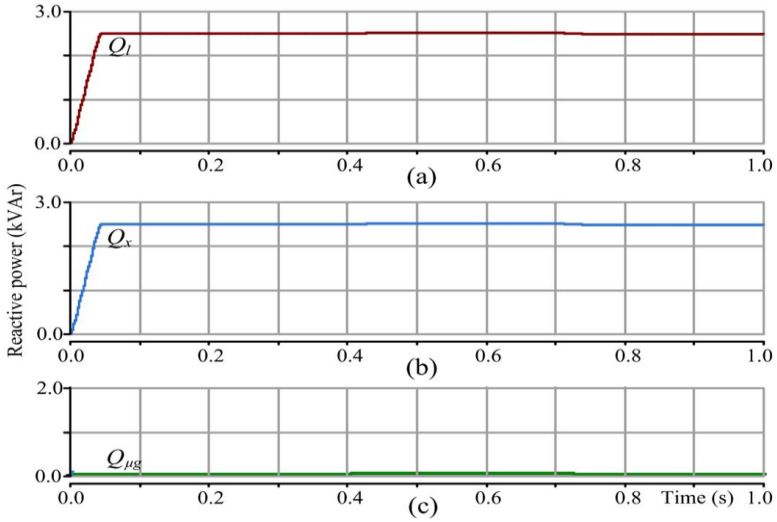

Fig.7. Reactive power sharing: (a) load reactive power; (b) reactive power supplied by AVSI; and (c) reactive power supplied by MVSI.

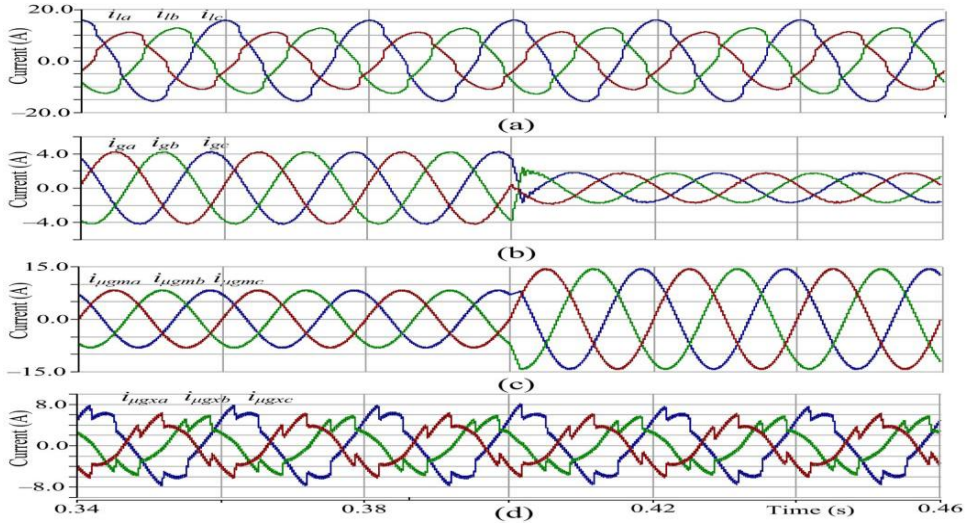

Fig. 8. Simulated performance of DVSI scheme: (a) load currents; (b) grid currents; (c) MVSI currents; and (d) AVSI currents in load currents.

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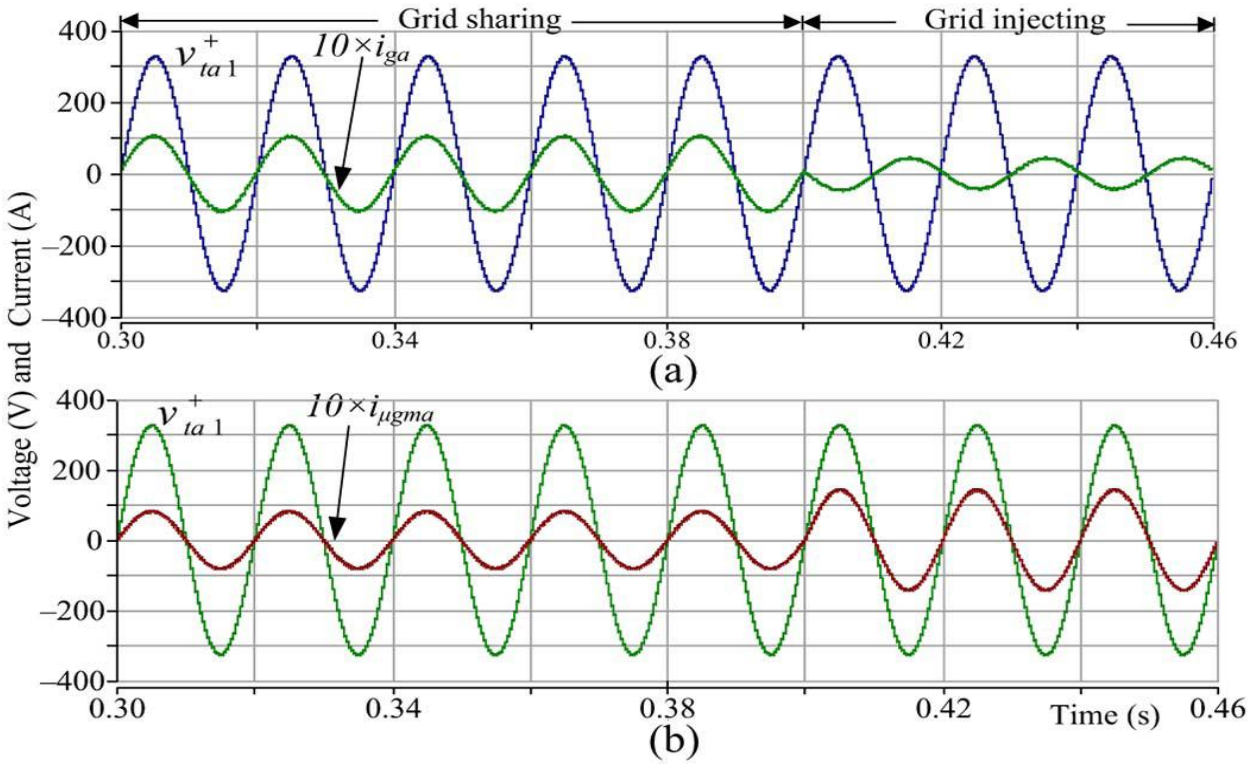

Fig.9. Grid sharing and grid injecting modes of operation: (a) PCC voltage

and grid current (phase-*a*) and (b) PCC voltage and MVSI current (phase-*a*). Fig. 9(a) shows the plot of fundamental positive sequence of PCC voltage (*v*+*ta*1) and grid current in phase-*a* (*iga*) during grid sharing and grid injecting modes. During grid sharing mode, this PCC voltage and grid current are in phase and during grid injecting mode, they are out of phase. Fig. 9(b) establishes that MVSI current in phase-*a* is always in phase with fundamental positive sequence of phase-*a* PCC voltage. The same is true for other two phases. Thus the compensation capability of AVSI makes the source current and MVSI current at unity power factor operation. The dc-link voltage of AVSI

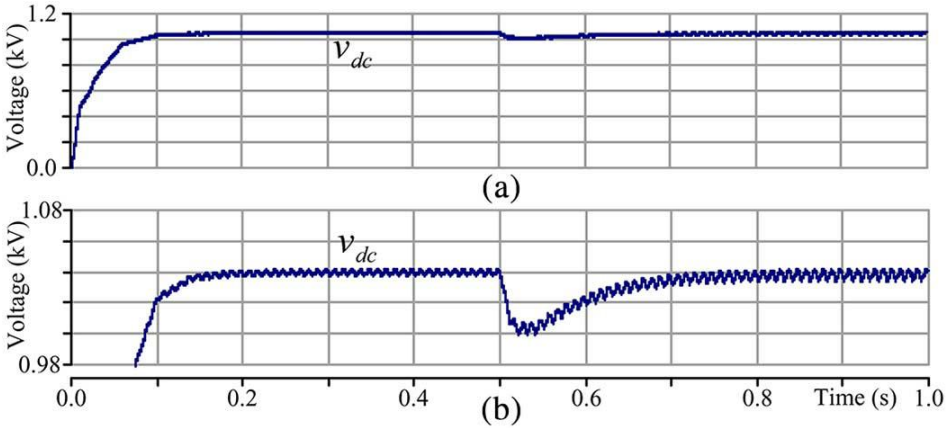

Fig.10. (a) DC-link voltage of AVSI and (b) zoomed view of dc-link voltage dynamics during load change.

is shown in Fig. 10(a) and (b). These figures indicate that the voltage is maintained constant at a reference voltage (*V*dcref) of 1040 V by the PI controller. All these simulation results presented above demonstrate the feasibility of DVSI for the load compensation as well as power injection from DG units in a microgrid.

TABLE II

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SYSTEM PARAMETERS FOR EXPERIMENTAL STUDY

Parameters	Values
Source voltage	50 V L–N (rms), 50 Hz
Feeder impedance	$R_g = 0.5\,\Omega$, $L_g = 1.0$ mH
Reference DC-link voltage of AVSI	$V_{dcref} = 220$ V
DC-link capacitance of AVSI	$C_1 = C_2 = 4700\ \mu$F
DC-link voltage of MVSI	$V_{dcm} = 150$ V
PI gains of DC-link voltage controller	$K_{Pv} = 80$, $K_{Iv} = 0.08$
Hysterisis band (h)	$\pm$ 0.15 A
Interfacing inductor (AVSI)	R_{fx}= 0.5 Ω, L_{fx}= 10 mH
Interfacing inductor (MVSI)	R_{fm}= 0.5 Ω, L_{fm}= 5 mH
Unbalanced linear load	$Z_{la} = 24 + j16\ \Omega$ $Z_{lb} = 36 + j16\ \Omega$ $Z_{lc} = 64 + j21\ \Omega$
Nonlinear load	3 ϕ diode bridge rectifier with a dc current of 2.4 A

VI. CONCLUSION

A DVSI scheme is proposed for microgrid systems with enhanced power quality. Control algorithms are developed to generate reference currents for DVSI using ISCT. The proposed scheme has the capability to exchange power from distributed generators (DGs) and also to compensate the local unbalanced and nonlinear load. The performance of the proposed scheme has been validated through simulation and experimental studies.

As compared to a single inverter with multifunctional capabilities, a DVSI has many advantages such as, increased reliability, lower cost due to the reduction in filter size, and more utilization of inverter capacity to inject real power from DGs to microgrid. Moreover, the use of three-phase, threewire topology for the main inverter reduces the dc-link voltage requirement. Thus, a DVSI scheme is a suitable interfacing option for microgrid supplying sensitive loads.

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