Gate All Around FET: An Alternative of FinFET for Future Technology Nodes

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ABSTRACT

Scaling of devices is reaching a brick wall because of short channel effects and quantum behavior of carriers at this scaled level. At this level, the quantum mechanics became more commanding over classical mechanics. To keep Moore's law alive, Gate All Around FET is a better candidate over FinFET and other existing sub 22 nm device architectures because of its gate coupling which tunes the channel more precisely and accurately. In GAA device architecture the SCE are minimized as compared to FinFET at same technology node. Physical device models ofquantum level and theircalibrated parameters usedto simulate devices below 14nm technology were discussed. In this paper the transfer characteristics, output characteristics, gain, mobility roll off, subthreshold slope, I_{ON}/I_{OFF} ratio and DIBL of GAAFET simulated. Also compared these SCE in squared channel GAA and Cylindrical Channel GAA Structures. Simulated result shows that the SCEs were significantly reduced in cylindrical GAAFET. DIBL and SS were found to be 78mV/dec and 71mV/V vs. 113mV/dec and 73mV/V in Cylindrical GAAFET, Square channel GAAFET respectively.

Keywords: ATLAS, FinFET, Gate All Around (GAA), Scaling, Short Channel Effects (SCEs).

I. INTRODUCTION

From past half century, Transistor is being continuously proven to be the most significant invention of engineering and is the backbone of every field. The secret to this much success lies in the fact that Transistor has followed a constant miniaturization trend initially predicted by G. Moore [1]. While it was a standard to have a feature size of 10 um in early days of MOSFETdevelopment [2], now the same is nearly 10 nm, and efforts are continuously made to shrink it more. This trend has allowed semiconductor industry to provide more and more features with reduced cost and power consumption. But, scaling has its own limitations, which further became more significant and challenging to rectify for feature size in Nanometer regime [3]. Device with feature sizesbelow 100 nm range suffers fromlateral SCEs such as dopant fluctuation, hot electron effect, carrier velocity saturation, drain induced barrier lowering (DIBL). Subthreshold Swing (SS), leakage current, etc. and vertical gate insulator tunneling[4] [5] [6] [7].

Due to fundamental physical limitations, the scaling of planer MOSFET was predicted to be limited to 15nm, butit has already ended with 32nm technology node due to difficulties in maintaining the gate coupling of device with planer structure.To minimise SCEs and to improve the device performance changes such as strained Silicon, Silicon on Insulator (SOI), high k insulator (HK), metal gate (MG), non-uniform doping, [8] [9] [10] [11] [12][13]has been suggested and utilised in device design.But, to maintain suitable electrostatic gate control over channel these innovations were not sufficient and many non-planer device architectures like Dual gate, Pi-gate, Omega Gate, FinFET/Tri-Gate were also proposed and investigated [14] [15] [16] [17]. But due to its

compatibility with semiconductor processing FinFET was the most successful [18]. FinFET was first introduced by Intel at the22nmnode and since then FinFET has becomemost dominating technology. But with continued scaling trend, Fin structure also suffers. As channel doping engineering has serious drawbacks for small devices of current generation [19] [20], an architectural change is apparently one of the promising solution.

Due to symmetry, Gate All Around (GAA) structure is theoretically the most suitable configuration from the gate electrostatic control point of view. In GAA FETs the insulating oxide and gate electrode both wrap around the channel.In this paper, we investigated the performance of GAAFET with the help of Silvaco TCAD tool. By changing various design parameters, a number of iterative simulations were performed, and effects of each parameter on device performance were observed. As expected the simulation shows that GAAFET with its four gates delivers much better gate electrostatic control over the channel.Even at 10nm and beyond, in GAAFET the SCEs are minimized and are fairly within acceptable limits. The ON to OFF current ratio of thedevice was also found excellent, making it power efficient and thus a solid option for portable devices.GAAFET's performance is further enhanced by minimizing corner effects i.e. by cylindrical channel.

II. DEVICE PHYSICS

Following the trend of shrinking device dimensions, we have reached upto/beyond sub-deca nm feature size. At this size, the quantum mechanics became dominant over classical mechanics. It became difficult to control these devices, and Quantum corrections must be considered for accurately simulating andmodelingthe behaviourof such devices. In current work, quantum effects were considered by selecting appropriate models and their calibrated parameters were used. All simulations were performed using ATLAS device simulator tool of Silvaco TCAD. Bohm Quantum Potential model (BQP), Energy balanced model for electrons (HCTE.EL), and Field dependent mobility model (FLDMOB) were used in all simulations to get accurate results. Fermi-Dirac distribution instead of Boltzmann distribution was used forthermal equilibrium of carriers for initial guess. The physical device models used in thesimulationare discussed below.

2.1 Bohm Quantum Potential Model

Quantum Potential models are originated from the hydrodynamic formation of the quantum mechanics. The concept of Quantum potential was first introduced by de Broglie and Madelung [21]. Later Bohmfurther developed this model [22] [23]. In these models, the wave function of particleis writtenin terms of its amplitude and phase. These are then substituted back into the Schrodinger's equation to derive the following coupled equations of motion for density (1) and phase (2).

$$\frac{\partial \rho(r,t)}{\partial t} + \nabla \cdot \left(\rho(r,t) \frac{1}{m} \nabla S(r,t) \right) = 0 \quad (1)$$

$$\frac{-\partial S(r,t)}{\partial t} = \frac{1}{2m} [\nabla S(r,t)]^2 + V(r,t) + Q(\rho,r,t) \quad (2)$$

Where, $\rho(r,t)$=$R^2(r,t)$ is the probability density, Q is the Bohm Quantum Potential (3), V is potential term from Schrodinger equation and S is the solution of Hamiltonian-Jacobian equation [22]. Equation 1 has the form of continuity equation. Equation 1 and equation 2are derived from Madelung transformation of the Schrodinger equation. These equations have the form of classical hydrodynamic equations with an additional potential

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derived by Bohm's interpretation of Quantum mechanics and is known as Bohm Quantum Potential (BQP). BQP model used in our simulation was developed for Silvaco by the University of Pisa and has two advantages over density gradient method. First, it has better convergence properties in many situations. Second, it can be calibrated against results from the Schrodinger-Poisson equation under conditions of negligible current flow. BQP in ATLAS takes the following form[26]:

$$Q = \frac{-h^2}{2} \frac{\gamma \nabla (M^{-1} \nabla (n^\alpha))}{n^\alpha} \quad (3)$$

Where,*Alpha* and *gamma* are twofitting parameters, M^{-1} is the inverse effective mass tensor and *n* is the electron (or hole) density. BQP method can also be used for the Energy balance and hydrodynamic models, where the semi-classical potential is modified by the quantum potential.

2.2 Energy Balance Transport Model

Simple Drift-Diffusion transport model has thelimitation of not introducing the energy (carrier temperature) as anindependent variable which makes it less accurate for deep submicron devices and too high gradients. So, for these devices, a higher order solution of general Boltzmann's Transport Equations (BTE) is required. Energy Balance Transport Model is a higher order solution to the general Boltzmann Transport Equation and consists of an additional coupling of the current density to the carrier temperature (or energy) model by introducing two new independent variables Tn and Tp, the carrier temperature for electrons and holes. The current density expressions from the drift-diffusion model are modified to include this additional physical relationship. The energy balance equations consist of an energy balance equation with the associated equations for current density and energy flux.For electrons, the Energy Balance Transport Model consists of [24]:

$$\text{div } S_n = \frac{1}{q} J_n E - W_n - \frac{3k}{2} \cdot \frac{\partial}{\partial t} (\lambda_n^* n T_n) \quad (4)$$

$$J_n = q D_n \nabla_n - q \mu_n n \nabla \psi + q n D_n^T \nabla T_n \quad (5)$$

$$S_n = -K_n \nabla T_n - \left(\frac{k \delta_n}{q}\right) J_n T_n \quad (6)$$

Where $T_n$represent the electron temperatures,J_n is current density (5), $S_n$is the flux of energy (6), μ_n is the electron mobilities, D_n is thermal diffusivity for electrons, W_n is the energy density loss rate for electrons, and K_n is the thermal conductivities of electrons.

III. DEVICE SIMULATION

In the current work, device structures were made with DEVEDIT3d and simulated with ATLAS device simulator of Silvaco TCAD. In BQP model,*Alpha* and *Gamma* parameters were set to 0.3 and 1.4 resp. for calibration against Schrodinger-Poisson solver to set isotropic effective masses of Silicon to 0.7 m_0. For solutions BLOCK iterative method was used, GUMMELwas used for initial guess, NEWTON RICHARDSON was used to speed up the calculations in iterations.
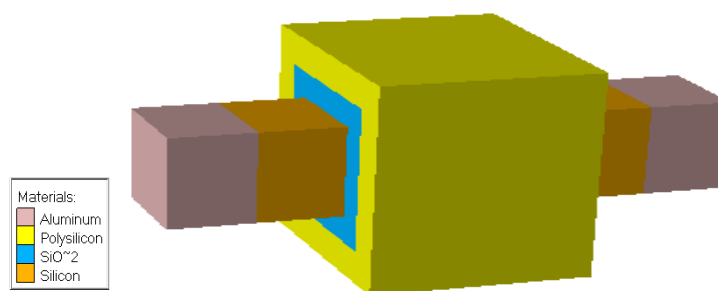
Fig. 1: Gate All Around Field Effect Transistor

Fig.1 shows the bird's eye view of the device structure simulated. The device is n-channel with SOI substrate. Poly-silicon was used as gatematerial, and Silicon dioxide (**SiO₂**) was used as theinsulating dielectric material. Other parameters are as follows: Gate length (**L_g**)=10nm, height (**H**) = 7nm, width (**W**)=7nm, Oxide thickness (**T**)=2nm. Source and Drain doping=$1e^{19}$atoms/cm^3 and doping profile set to Gaussian with Z roll-off of 0.5nm, Channel doping=$1e^{14}$ atoms/cm^3. These values are taken as standard and are same throughout the paper unless mentioned.

IV. RESULTS AND DISCUSSION

Fig.2 shows the transfer characteristics of GAAFET device. These transfer characteristics were obtained at fixed Drain voltages (V_d) of 0.05V and 0.5V. At each (V_d), theGate voltage (V_g) was swiped from 0 to 0.8V. Drain current is plotted along Y-axis in $\log_{10}(I_d)$ and Gate voltage along theX axis in Volts.

Output characteristics of GAAFET are plotted in Fig. 3. Three plots of **I_d** (along Y axis in Amperes) vs.**V_d** (along the X axis in Volts) are plotted at Gate bias of 0.45V, 0.55V, and 0.60V respectively. At each Gate bias (**V_g**) Drain voltage (**V_d**) was varied from 0 to 0.75V.

Detailed results of GAAFET simulation are summarized in **Table I**. Threshold voltage (**V_{th}**) was calculated from the Transfer characteristics curve at a fixed drain current of $0.3e^{-7}$A [25]. **Beta** is the gain and **Theta** is Level-3 mobility roll off for SPICE simulation. Sub-threshold swing (**SS**) is in mV/decade. **DIBL** was defined as thedifference in threshold voltage when drain voltage varied from 50mV to 0.5V. **I_{ON}/I_{OFF}** ratio was determined by extracting minimum and maximum current from the **I_d**vs.**V_g** curve.
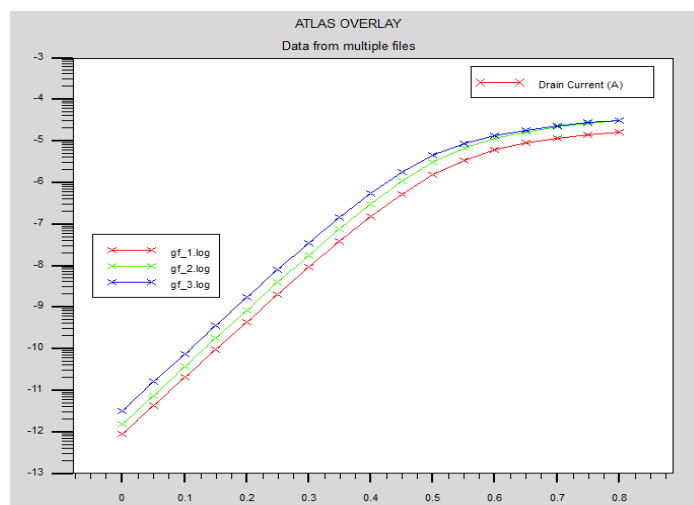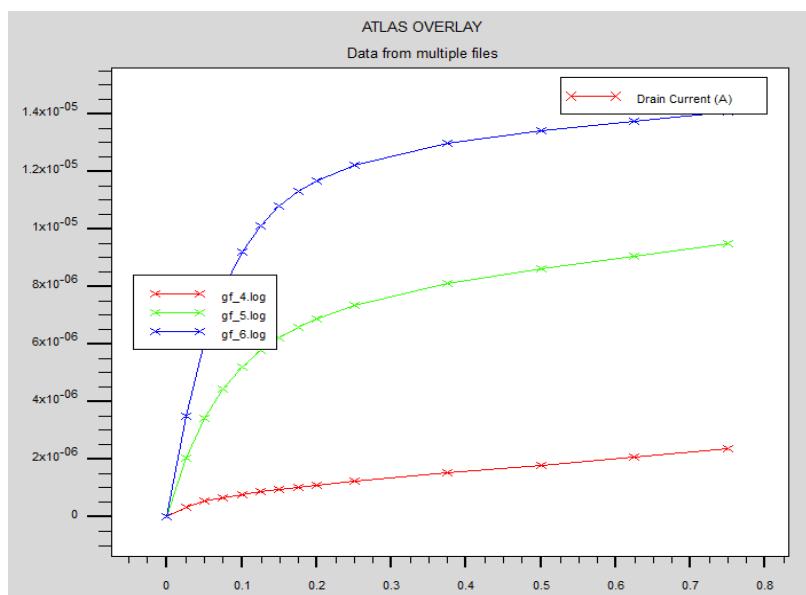

Fig. 2: Transfer characteristics of GAAFET

Fig. 3 Output characteristics of GAAFET

Table I: Extracted Results from GAAFET Simulation

Parameter Name	Vg=0.02V	Vg=0.1V	Vg=0.5V
V_{th}	0.420	0.398	0.368
Beta	0.00116	0.00051	0.0019
Theta	0.83	0.84	0.77
SS	0.0735	0.0726	0.0722

I_{ON} to I_{OFF} ratio of GAAFET was found $1.9e^7$, which is excellent considering the small dimensions of thedevice.DIBL of GAAFET was calculated 113mV/V, which is within acceptable limits for a 10nm channel device. The variation of SS and DIBL with oxide thickness is shown in Fig. 4 and Fig. 5 respectively.As seen **SS**decreased from 85mV/V to 73mV/V when gate oxide thickness was reduced from 3nm to 1nm and **DIBL** decreased from 159mV/dec to 71mV/dec when gate oxide thickness was reduced from 3nm to 1nm.
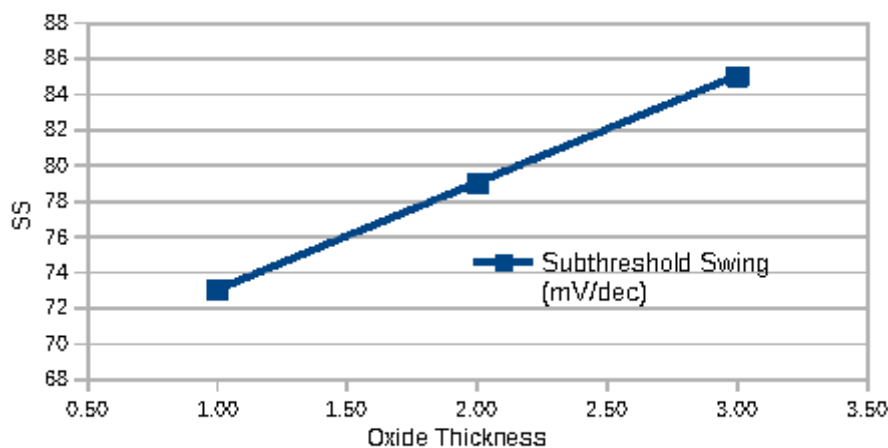
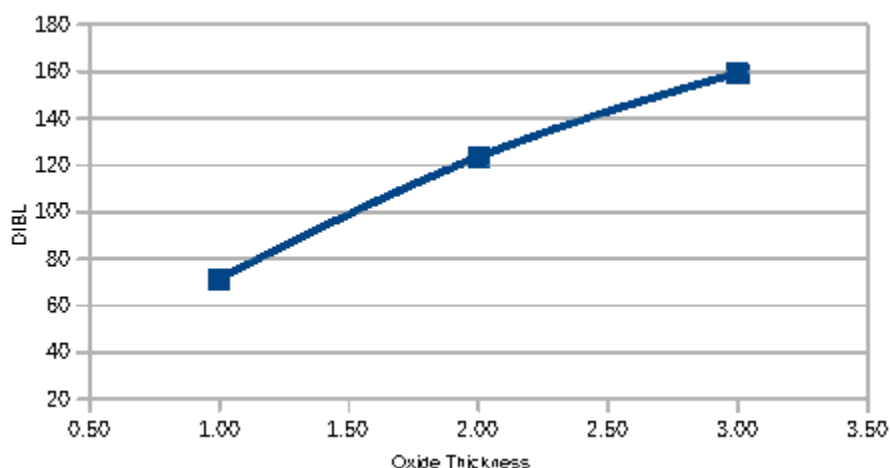

Fig. 4: SS versus Oxide thickness

Fig. 5: DIBL versus Oxide thickness

GAA MOSFETs generally suffer from corner effects. As shown in Fig. 6, the large electric field gathers around the edges of each channel in square GAA structure. The gate electrodes cannot sharply control the channels. This may cause short-channel effects. To observe the performance of corner effect free device the shape of GAA structure was changed to ideal cylindrical GAA structure and simulation was performed again.
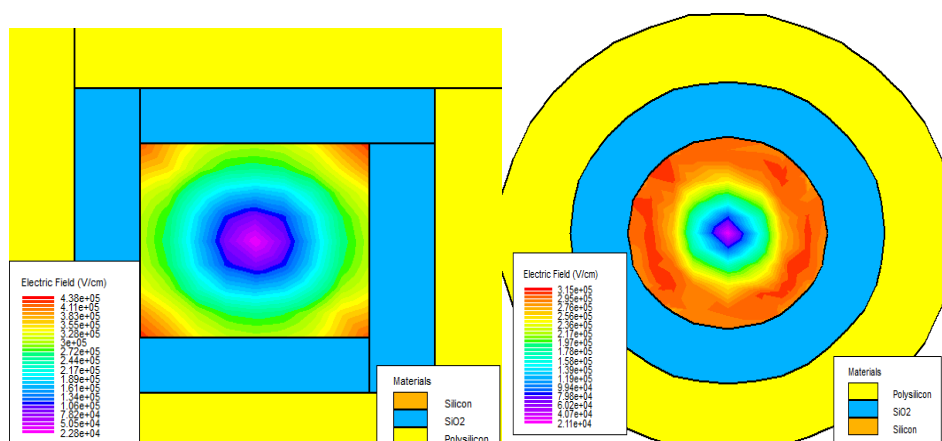

Fig. 6: Corner effects in square channel GAAFET

The diameter of thechannelwas kept 7nm equal to the channel height and width of square channel GAAFET, oxide thickness was set to 2nm. The structure of ideal cylindrical channel GAAFET is shown in Fig. 7.
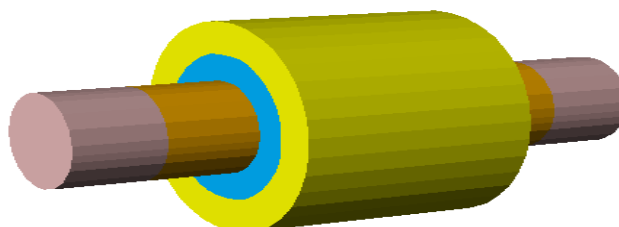

Fig. 7: Ideal cylindrical channel GAAFET

Due to its symmetrical nature, the cylindrical shape of the gate and channel eliminate the corner effects. The electric field as shown in the Fig. 6, is uniformly spanned in the circular rings within the channel. Cylindrical

channel shape provides better gate coupling and as expected the overall performance of the GAAFET was improved. The comparative results of simulations are summarized in Table II. In square channel GAAFETs the electric field near the corners of the channel was undesirably high which was resulting into high off current but in cylindrical channel device the off current was significantly reduced due to the strong and symmetrical electrostatic gate control over the channel which also improved the I_{on}/I_{off}ratio of the device. The relatively low saturation current in cylindrical channel GAAFET is justifiable by the fact that relative cross-section area of a7nm diametric cylinder is small considering square of 7nm by 7nm. Also, these I_{dss} values are extracted at V_g=0.60V,and there is a difference in $V_{TH}$of both devices. The SCEs were also remarkably reduced in cylindrical GAAFET. DIBL and SS were found78mV/dec and 71mV/V in Cylindrical GAAFET which were 113mV/dec and 73mV/Vrespectively in square channel GAAFET.

Table II. Extracted Result of Square and cylindrical channel GAAFET Simulations

Parameter Name	Square Channel GAAFET	Cylindrical Channel GAAFET
I_{dss}	$1.72e^{-5}$	$8.77e^{-6}$
V_{TH}	0.42	0.45
Beta	0.00116	0.00091
Theta	0.82	0.74
SS	0.073	0.071
DIBL	0.113	0.078
I_{on}/I_{off}	$1.8e^7$	$6.4e^7$

Fig. 8 shows the channel inversion in thesquare channel and cylindrical channel GAAFETs. It is seen that in the cylindrical channel device very strong and symmetrical volume inversion is achieved compared to square channel device.
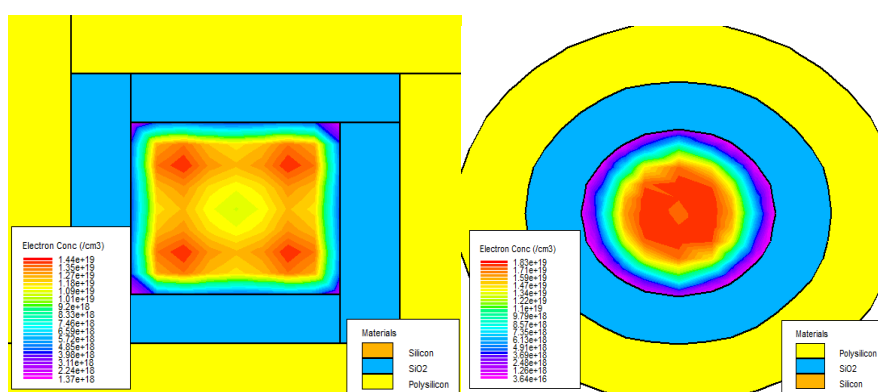

Fig. 8:Channel inversion in thesquare channel and cylindrical channel GAAFETs; cylindrical channel GAAFET has more symmetrical and strong volume inversion.

VI. CONCLUSION

The 3D simulation performed shows that even in deep sub-micron regime GAA structure has very good performance. The effect of theadditional gate in GAA structure accountsfor the enhanced performance of thedevice by providing better gate control over thechannel. As seen from DIBL and SS parameters, GAAFET is robust to Short Channel Effects and can replace the Fin structure in future nodes. The ON to OFF current ratio of the cylindrical channel GAAFET is approximately five times better than that of the square channel GAAFET which proves that the cylindric shape of thechannel can further improve the performance of GAAFET making it ideal GAA structure froma performance point of view and for power efficient portable devices.

VI. ACKNOWLEGEMENT

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