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DESIGN AND IMPLEMENTION OF LOW POWER SRAM CELL USING SELF-CONTROLLABLE VOLTAGE LEVEL

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ABSTRACT

Memories are critical parts of most of the digital gadgets and therefore reducing energy intake of memory may be very essential in improving the performance, efficiency and stability. Static Random Access Memory (SRAM) is faster and greater suitable than other such as Dynamic Random Access Memory (DRAM) or Flash Memories. The power performance and speedof SRAM are the most vital difficulty for minimizing the strength all through read and write operations. The primary cause of this paper is to provide anEnergyEfficient Low Power SRAM cell and right here method called "Self Controllable Voltage Logic" are used and numerous processes are mentioned to reap the higher overall performance. Simulation result of SRAM cellular with decreased strength is carried out using Tanner EDA tool.

Keywords: ISVL,Low Power,LSVL, SRAM, SVl, USVL.

I. INTRODUCTION

Random-Access Memory (RAM) is a type of computer facts storage which stores frequently used application instructions to increase the general speed of a system. A random-access memory device lets in records objects to be read or write in almost the same quantity of time no matter the physical location of statistics in the reminiscence. Each bit in an SRAM is stored on 4 transistors that shape cross coupled inverters. With increased tool variability in nanometers scale technology, SRAM will become an increasing number of vulnerable to noise sources 6T SRAM is a bistable device includes back to back related inverters (M1, M2, M3, and M4) alongsideaccess transistors(M5 and M6) being separately related to 2 complementary bit traces BL and BLb get entry to gadgets which permit to access to inner node of the cell. Two back to back inverters store two states 0 and 1. SRAM cells include a latch and, it's called static memory due to the cell data is saved so long as power is become on and refresh operation isn't required for the SRAM [8]. There are many power reduction techniques such as multi threshold voltage CMOS (MTCMOS) and variable threshold CMOS (VTCMOS) [10]. In the first technique power has been reduced. Effectively by use of high V_t MOSFET switches which disconnects the power supply. If this is applied with memories and flip- flops it has a drawback of not retaining data. In the other technique variable threshold voltage CMOS (VTCMOS) is used that reduces Power by increasing the substrate-biases [2]. The drawbacks for this technique is large area problem as well as power dissipation. So a self-controllable voltage level (SVL) technique is proposed where the load circuits

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in active mode allows full supply voltage and decreased supply voltage appears to be proficient for reducing gate leakage currents [11] as well.

II. 6T SRAM

SRAM cell is made up of six MOSFETs. Each bit in an SRAM is stored on two cross-coupled inverters that formed by four transistors (M1, M2, M3, M4). This storage cell has two stable states which are used to denote 0 and 1. Two additional access transistors serve to control the access to a storage cell during read and write operations [7].

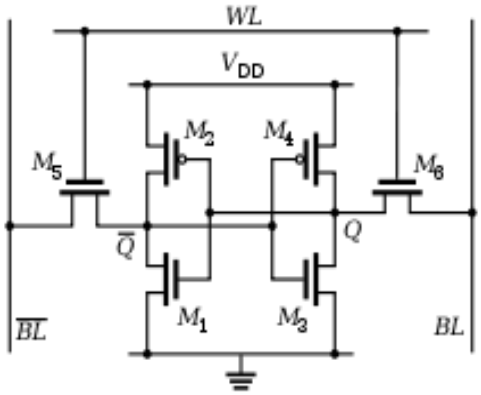

Fig.1: Circuit diagram of 6T SRAM

2.1 SRAM Operation

An SRAM cell has 3 distinct states: standby (the circuit is idle), reading (the data has been requested) or writing (updating the contents). SRAM operating in study mode and write modes must have "readability" and "write stability", respectively. The three exceptional states work as follows:

2.2 Standby

If the word line is not asserted, M_5 and M_6 the access transistors disconnect the cell from the bit lines. The two cross-coupled inverters formed by the four transistors $M_1 – M_4$ will continue to reinforce each other as long as they are connected to the supply.

2.3 Reading

In idea, reading handiest requires maintaining the word line WL and reading the SRAM cell state by a single access transistor and bit line, e.g. M_6, BL. Nevertheless, bit lines are relatively long and have large parasitic capacitance. To speed up reading, a more complicated process is used in practice: The read cycle is started by precharging each bit lines BL and BLb, i.e., driving the bit lines to a threshold voltage (midrange voltage between logical **1** and **0**). Then asserting the word line WL enables each of the access transistors M_5 and M_6, which causes the bit line BL voltage to either slightly decrease (bottom NMOS transistor M_3 is ON and top PMOS transistor M_4 is off) or increase (top PMOS transistor M_4 is on). It should be noted that if BL voltage increases, the BLb voltage decreases, and vice versa. Then the BL and BLb lines will have a small voltage difference between them.

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2.4 Writing

The write cycle begins through applying the value to be written to the bit lines. If we wish to write a 0, we would apply a 0 to the bit lines, i.e. setting BLb to **1** and BL to **0**. This is much like to applying a reset pulse to an SR-latch, which causes the flip flop to change state. A **1** is written by way of inverting the values of the bit lines. WL is then asserted and the value that is to be saved is latched in. This works because the bit line input-drivers are designed to be much stronger than the relatively weak transistors in the cell itself so they can easily override the previous state of the cross-coupled inverters. In practice, access NMOS transistors M_5 and M_6 have to be stronger than either bottom NMOS (M_1, M_3) or top PMOS (M_2, M_4) transistors. This is easily obtained as PMOS transistors are much weaker than NMOS when same sized. Consequently when one transistor pair (e.g. M_3 and M_4) is only slightly overridden by the write process, the opposite transistors pair (M_1 and M_2) gate voltage is also changed. This means that the M_1 and M_2transistors can be easier overridden, and so on. Thus, cross-coupled inverters magnify the writing process.[7]

III. PROPOSED METHOD

3.1 Self-Controllable Voltage Level (SVL)

SVL is the acronym for Self controllableVoltage Level. SVL technique is used to reduce leakage strength for the duration of standby mode of operation i.e. when clock=0. SVL technique uses a PMOS and a NMOS transistor in parallel as pull up network in addition to pull down network. Pull up transistors gate isconnected with complement of clock signal and pull downtransistors gate terminal is attached with clock .Thisapproach to reduce leakage power makes use of a clock signal asthe manipulate signal to govern supply voltage .As a result the call Self controllable Voltage Level Logic is justified.[1]

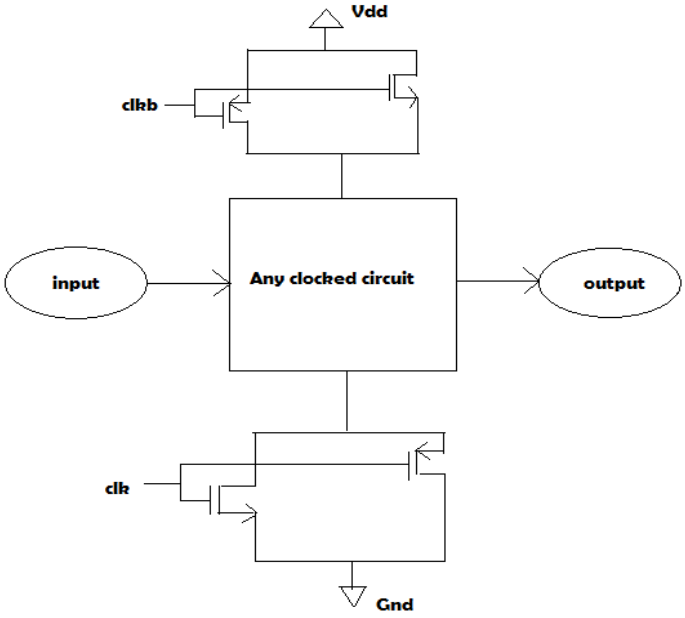

Fig.2: SVL circuit [6]

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3.2 Improved Self-Controllable Voltage Level (ISVL)

3.2.1 Upper Self-Controllable Voltage Level(USVL)

In Upper Self-Controllable Voltage Level circuit (USVL) the impedance of MOS transistor increases with the width of transistor. $PMOS_1$ having width means it offers high resistance in the path between V_{dd} and V_d. The $NMOS_1$ and $NMOS_2$ form a read and write working in normal mode of a cell whereas

$NMOS_2$ act as resistor to reduce current in active mode by connecting upper SVL circuit and reduced leakage power. [1]

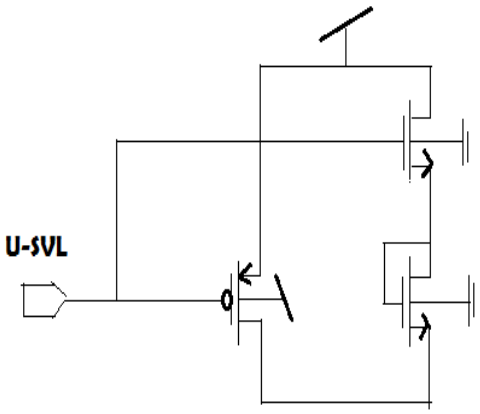

Fig.3: Upper SVL circuit

3.2.2 Lower Self-Controllable Voltage Level (LSVL)

In Lower self-controllable voltage level circuit (LSVL) the impedance of MOS transistor increases with the width of transistor. $NMOS_1$ having width means it offers high resistance in the path between $V_{dd}$and V_d. The $NMOS_3$ work in SVL mode and $PMOS_2$ and $PMOS_3$ work in normal mode of the cell. $PMOS_2$ act as resistor to reduce leakage power. The lower SVL circuit not only supply power to active load circuit through the on n-SW and also supplies V_{ss} to the standby load circuit through p-SWs.

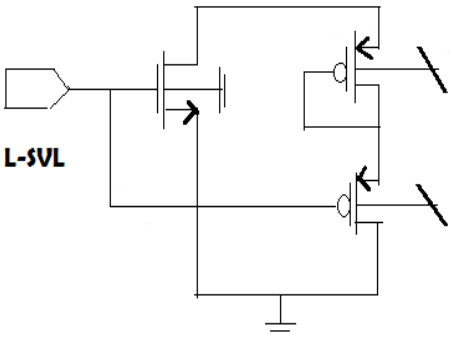

Fig.4: Lower SVL circuit

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IV. IMPLEMENTATION & CIRCUIT SIMULATION

In this paper normal 6T SRAM, 6T SRAM with SVL and 6T SRAM with Improved SVL are simulated on Tanner EDA tool at 180nm technology with different supply voltages and the results are obtained.

3.3 SRAM

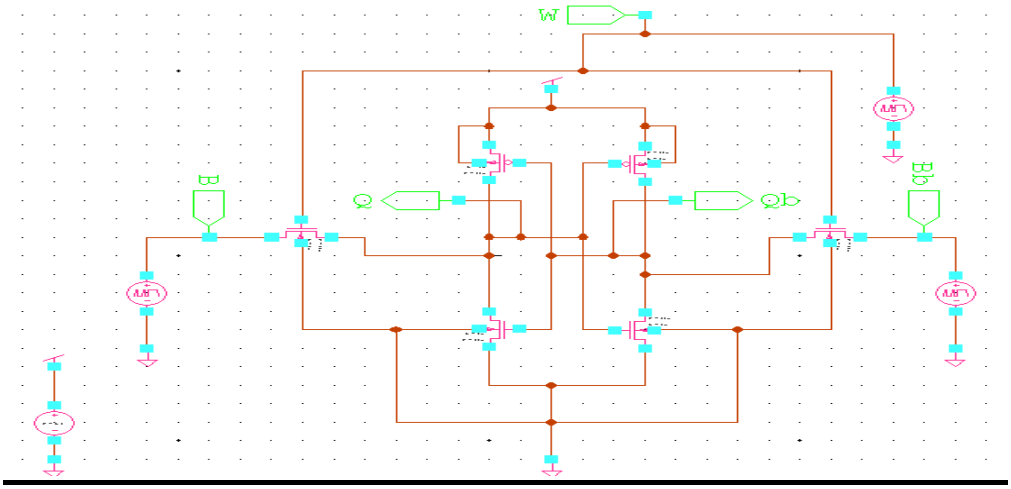

Fig.5: Circuit of 6T SRAM

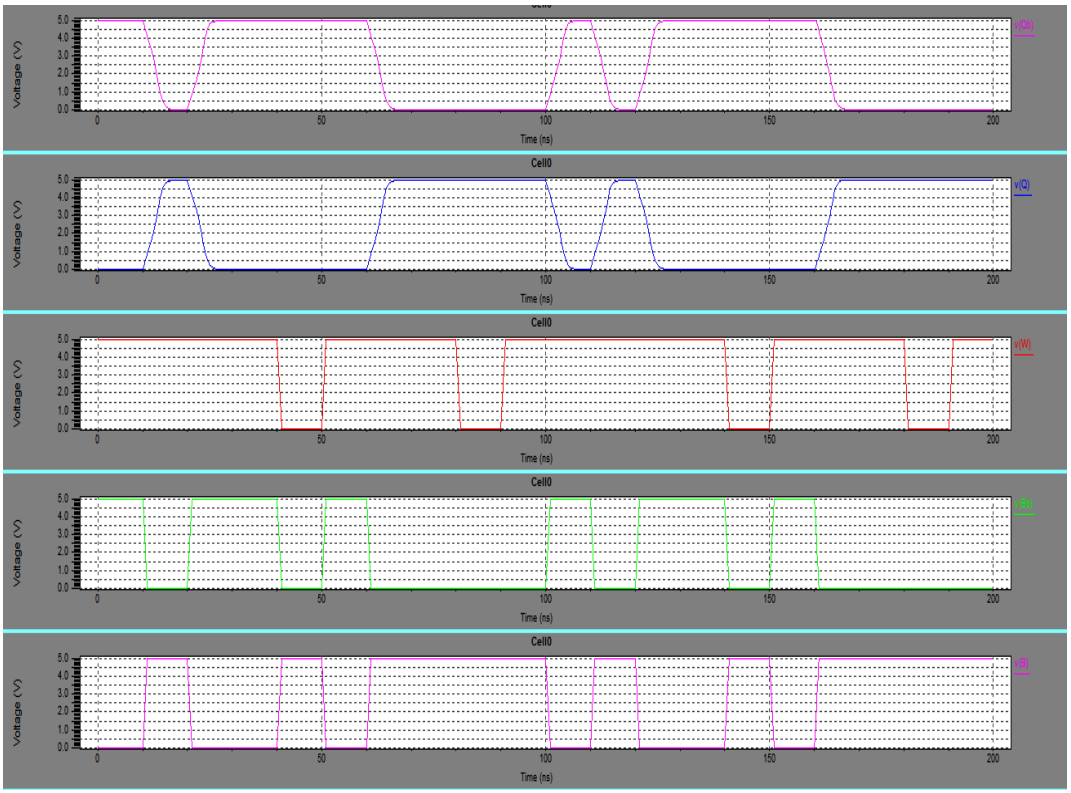

Fig.6: Output waveform of 6T SRAM

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Table 1: Simulation result of SRAM cell

Power supply(V)	Power(w)	Delay(s)
0.7	2.083400e-004	1.0640e-008
1.8	3.130410e-004	1.0640e-008
5.0	5.402156e-004	1.0640e-008

3.4 SRAM with SVL Technique

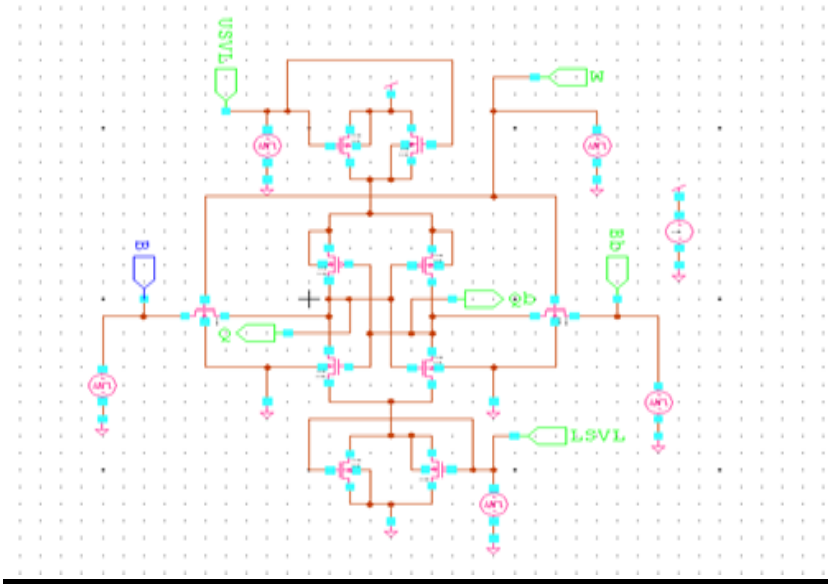

Fig.7: Circuit of 6T SRAM using SVL technique

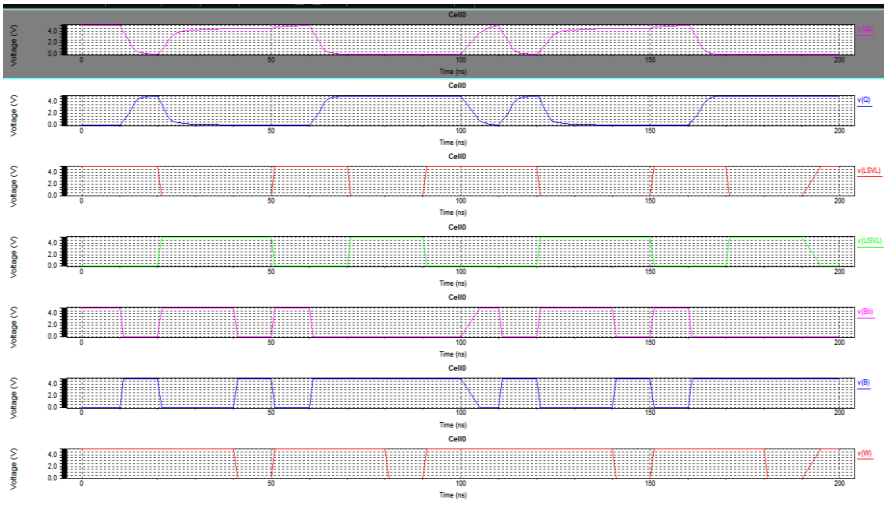

Fig.8:Output waveform of 6T SRAM using SVL technique

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Table 2: Simulation result of SVL SRAM cell

Power supply(V)	Power(w)	Delay(s)
0.7	1.446870e-004	1.1308e-008
1.8	2.496931e-004	1.1671e-008
5.0	2.888867e-004	1.3230e-008

3.5 SRAM with ISVL Technique

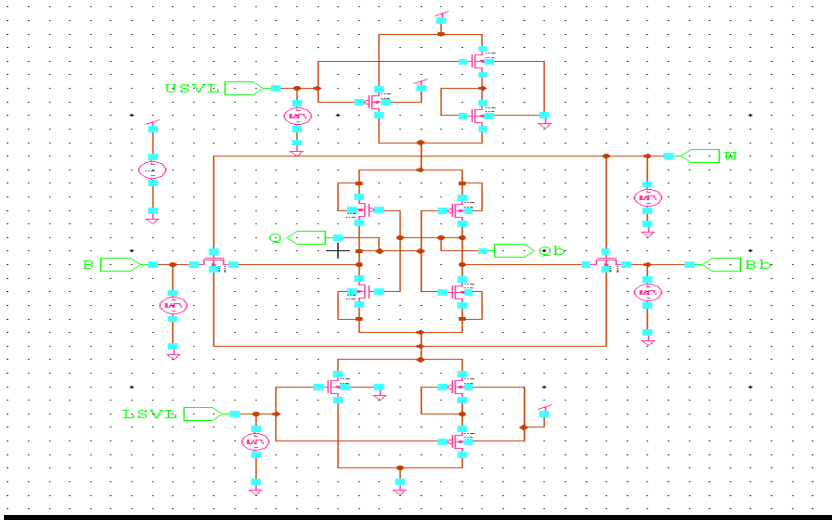

Fig.9: Circuit of 6T SRAM using ISVL technique

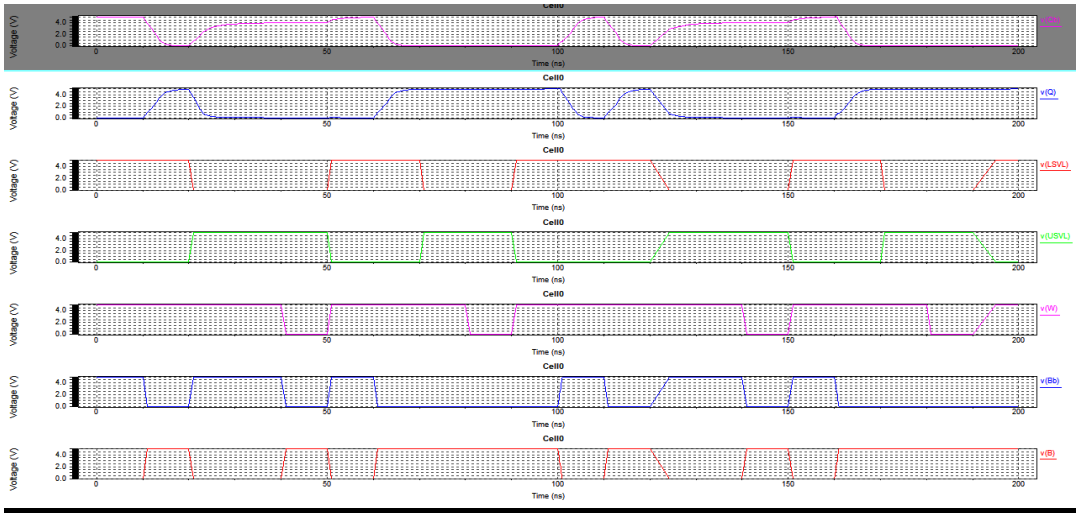

Fig.10: Output waveform of 6T SRAM using ISVL technique

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Table 3: Simulation result of ISVL SRAM cell

Power supply(V)	Power(w)	Delay(s)
0.7	1.389026e-004	1.1541e-008
1.8	2.261862e-004	1.1813e-008
5.0	2.808951e-004	1.2908e-008

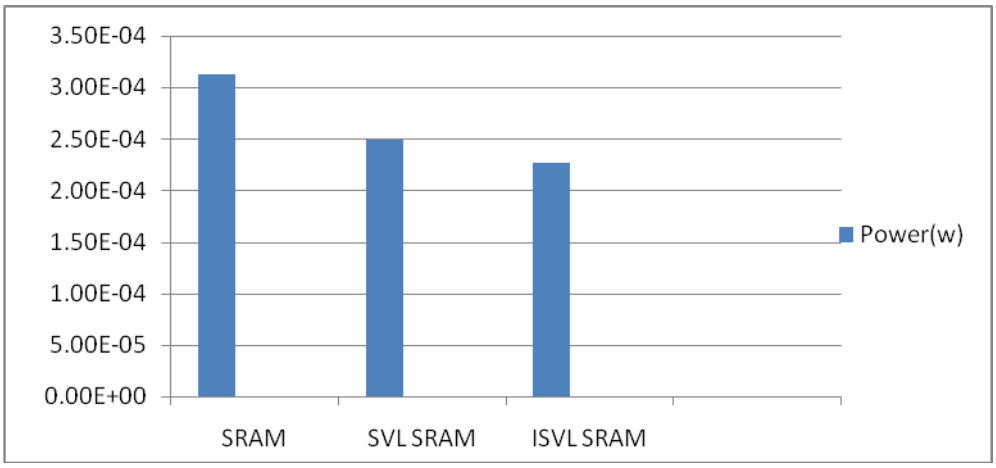
IV. RESULT

This section deals with the comparison of the entire SRAM cellin terms of Average Power consumed and delay. The results were simulated using TSPICE tanner tool at 180nm technology.

Table 4: Comparison between techniques at 1.8v

Technique	Power(w)	Delay(s)
SRAM	3.130410e-004	1.0640e-008
SVL SRAM	2.496931e-004	1.1671e-008
ISVL SRAM	2.261862e-004	1.1813e-008

From the above comparison table it is clear that the improved Self-Controllable Voltage Level (ISVL) technique hasminimum averagepower consumption.



Graph 1. Shows the average power consumption

V. CONCLUSION

A self-controllable voltage level (SVL) circuit, which overcome the disadvantages of the other low power techniques like MTCMOS and VTCMOS. In SVL circuit drain-source voltage is dynamically reduced and a substrate bias in stand by load circuit is increases. Fromthe above simulation results it is clearly seen that the

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reduction in the power consumption by Improved Self-Controllable Voltage Level **(**ISVL) with Self-Controllable Voltage Level **(**SVL) technique is near about 80%. The simulation results are carried out on Tanner EDA tool. 6T SRAM using Improved SVL techniques has better performance than the previous designs.

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