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DESIGN AND FPGA IMPLEMENTATION OF HIGH SPEED VEDIC MULTIPLIER

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ABSTRACT

Multiplication is an operation much needed in Digital Signal Processing for various applications. This paper puts forward a high speed Vedic multiplier which is efficient in terms of speed, making use of Urdhva Tiryagbhyam, a sutra from Vedic Math for multiplication and Kogge Stone algorithm for performing addition of partial products and also compares it with the characteristics of existing algorithms. The below two algorithms aids to parallel generation of partial products and faster carry generation respectively, leading to better performance. The code is written in Verilog HDL and implemented on Xilinx Spartan 3 and Spartan 6 FPGA kit using Xilinx ISE 9.1i. The propagation delay of the implemented architecture is obtained to be 28.699ns and 15.752ns respectively.Keywords: Compressed sensing, Energy detector, Narrowband interference, ultra-wideband Communication field .

Keywords: Urdhva Tiryagbhyam;

I. INTRODUCTION

Vedic Mathematics is an ancient system of math practiced during Vedic age which was reconstructed by Jagadguru Swami Sri Bharati Krishna Tirthaji Maharaja[1] between 1911 and 1918 from certain Sanskrit manuscripts. It is perhaps the most refined and efficient mathematical system possible. One of such efficient technique has been employed to enhance the design of a multiplier. Multipliers are the key blocks of a Digital Signal processor. Multiplication is the key aspect, whereby improvement in computational speed of multiplication decreases the processing time of Digital Signal Processors. Convolution, Fast Fourier transforms and various other transforms make use of multiplier blocks.

A faster method for multiplication based on ancient Indian Vedic mathematics is studied in this paper. Among various methods of multiplications in Vedic mathematics, Urdhva Tiryagbhyam is efficient [2]. Urdhva Tiryagbhyam is a general multiplication formula applicable to all cases of multiplication. For addition of partial

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products in the multiplier Kogge Stone algorithm is used and realized. The code is written in Verilog HDL[3] and synthesized using Xilinx ISE 9.1i and implemented on Spartan 3 and 6 FPGA devices.

II. URDHVA-TIRYAKBHYAM SUTRA (VERTICALLY AND CROSSWISE)

In this section we propose a Vedic multiplication technique which is based on "Urdhva-Tiryakbhyam – Vertically and crosswise" sutra. Vedic multiplier technique consists of generation of parallel partial products and addition operation simultaneously. This algorithm can be used for 2×2, 4×4, 8×8, 16×6....N×N bit multiplications. In this method sum and their partial products are calculated in parallel hence Vedic multiplier does not depend upon the processor clock frequency and reduces the power dissipation. The use of "Urdhva-Tiryakbhyam sutra" for multiplication operation reduces the latency of a multiplier unit by introducing concurrent computing of partial products. The main advantage of the Vedic multiplier is that it reduces delay as well as power when compared with the exiting multipliers. To illustrate this technique, let us consider two decimal numbers 525 and 786 and Steps of multiplication are shown in Fig.

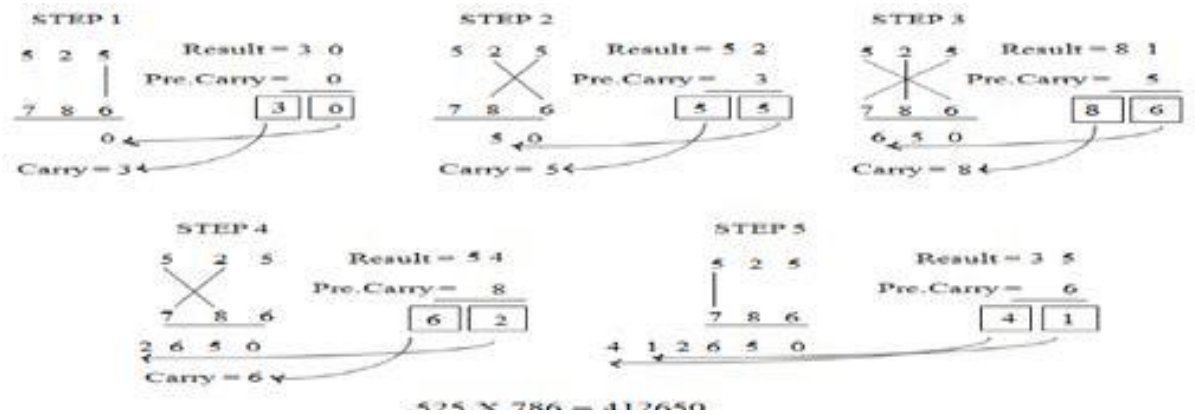

Fig1. Four bit multiplication using 'UT' sutra

S0 is obtained by multiply the least significant bits of the multiplicand and multiplier[4]. Numbers on both sides of the line are multiplied and added with carry from previous step in the last case. This generates one of the bits of the result sum and a carry. This carry is added in the next step hence the process goes on.

III. CONCLUSION LITERATURE CITED

The speed of the multiplier is decided by the latency of the circuit. The latency count is reduced from 18 to 5 that is 72.22% which is lesser with respect to the Dadda multiplier. The power dissipation at various frequencies (100MHz and 400MHz) at constant power supply 1.0v is investigated[5]. The power dissipation reduced in proposed architecture due to use of modified carry select adder as compared to the Dadda multiplier. Result shows that the proposed architecture is more efficient in terms of the speed and power compared to the existing one. Result shows that proposed 16x16 bit Vedic multiplier has leakage power consumption 2.49mw, PDP is

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4.43pj, delay is 0.73ns and average power dissipation is 6.08mw.The simulation results of proposed 16x16 bit Vedic multiplier are carried out with 1.0v at 1GHz frequency.

IV LITERATURE CITED

In conventional method, partial products are summated only after every partial product is obtained Whereas, in Vedic technique, partial products are obtained vertically as shown in the figure above and simultaneously once all the elements of a column are obtained, respective partial products are added. Hence, leads to advancement in speed over the conventional method..

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