International Journal of Advance Research in Science and Engineering
Vol. No.5, Issue No. 11, November 2016
www.ijarse.com
IJARSE
ISSN (O) 2319 - 8354
ISSN (P) 2319 - 8346

11 Level Inverter with Less Number of Switches

MubashraSazda Khan

SATI Vidisha (M.P.)

ABSTRACT

A multilevel inverter is a device which can produce desired alternating voltage levels as an output if multiple low level DC voltages are used at input. Cascaded multilevel inverter topology is most widely used because it has lesser harmonics and less switching stresses. On the other hand, cascaded topology uses high number of switches which leads to high heat losses, large size and cost. In this paper, a new configuration of cascaded multilevel inverter is presented. This configuration contains less number of switches due to which it produces fewer harmonic and also the overall cost is reduced. Four different Pulse width modulation techniques are compared. Simulation study in MATLAB/Simulink is used to confirm the validity of the proposed method.

I. INTRODUCTION

Now-a-days power electronic devices are industrial application. They are also used for conversion and control of electric power. Basically inverters are power electronics device which converts DC power to AC power. Traditional Inverters produces alternating staircase like output waveforms which contains high amount of harmonics. And therefore need of multilevel inverter is generated. Also it is easy to use multilevel inverters than using multiple power lines. The most important use of multilevel inverter technology is in medium to high voltages. This paper presents a configuration to generate 11 level output with less THD. Four different PWM methods namely, Inphase disposition, Anti-phase disposition, Carrier overlap and variable frequency methods are used to produce gating pulses.

The idea of multilevel inverters was first invented in 1975. The term multilevel starts with the 3 level inverter and further several multilevel inverters was developed. Unfortunately multilevel inverters have some cons. One of the biggest disadvantages is that it requires large number of power switches which makes the circuit complex and expensive. There are basically three types of MLI-

1. Diode clamped MLI
2. Capacitor clamped MLI
3. Cascaded H-bridge (where H stands for Hybrid).

The Cascaded H-bridge topology contains less number of switches as compared to diode and capacitor clamped MLI. It is made by connecting single phase inverter in series with separate DC sources for each unit. The pair of capacitor and switches is an H-bridge and provides input DC voltage for each H-bridge. These H-bridge cells

IJARSE
ISSN (O) 2319 - 8354
ISSN (P) 2319 - 8346

generate three different voltages and they are zero, positive DC and negative DC. Its advantage is that it has less number of components then other two MLI and hence this configuration is used.

The output voltage is given by

$V_o = V_1 + V_2 + V_3 + \ldots\ldots V_n$

In case of symmetric inverter all DC voltages are equal to $V_{dc\ and}$ number of voltage steps is as follows:

$N_{step} = 2n + 1$

Where n is number of full H-bridge and therefore the maximum output voltage is given by:

$V_{omax} = n * V_{dc}$

In case of asymmetric inverter the DC sources ae not equal to V.

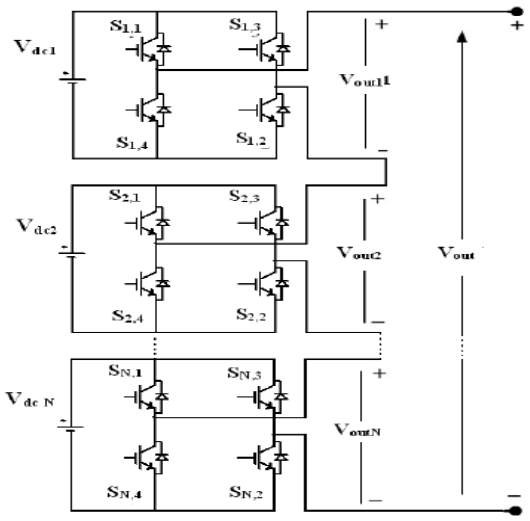

Fig 1: *Configuration of Cascaded Multilevel Inverter*

This paper presents a single phase inverter which has 8 switches and 3 DC voltage sources. A three phase configuration can be obtained by connecting three single phase inverter to a star connected resistive load and common earth point. Four different PWM methods are used to evaluate the performance of the inverter

II. SUGGESTED CONFIGURATION AND ITS SWITCHING

The proposed circuit consists of eight switches and three DC voltage sources per phase as shown in Fig 2. Four switches in left hand side are used to produce positive half cycle output waveform and the other four are used to produce the output waveform of negative half cycle. The three DC voltages are as V_{dc} ,$2V_{dc,}$ $2V_{dc}$ and they are connected in series to generate a 11 level output voltage.

IJARSE
ISSN (O) 2319 - 8354
ISSN (P) 2319 - 8346

As per the switching point of view we have to turn on four switches at a time to produce one output level. For example if we want to generate +5Vdc voltage level then we need to turn on switches S1 S3 S1' S4'. For +4Vdc we need to turn on S3 S1' S2' S4'. In the same way all the difeerent DC output voltages are generated. Table 2 Shows a Table which gives the switching details of all the eight switches.

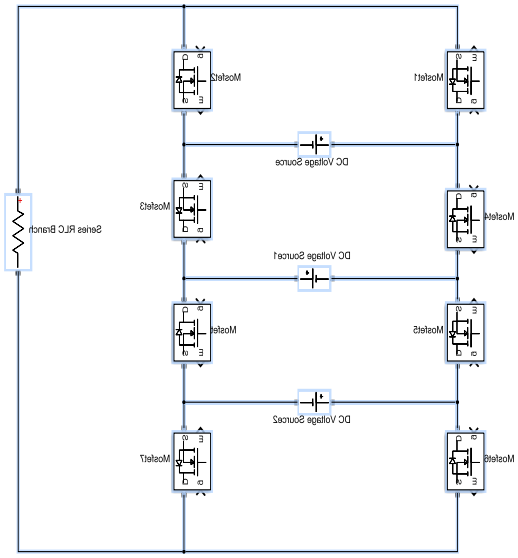

Fig 2: *Proposed Topology for single phase inverter*

Table 1: *Switching details of 11 level inverter*

Output voltage	S1	S2	S3	S4	S1'	S2'	S3'	S4'
+5V_{dc}	1	0	1	0	0	1	0	1
+4Vdc	0	0	1	0	1	1	0	1
+3Vdc	1	0	1	1	0	1	0	0
+2Vdc	1	1	1	0	0	0	0	1
+Vdc	1	0	0	0	0	1	1	1
0	0	0	0	0	1	1	1	1
-Vdc	0	1	1	1	1	0	0	0
-2Vdc	0	0	0	1	1	1	1	0
-3Vdc	0	1	0	0	1	0	1	1
-4Vdc	1	1	0	1	0	0	1	0
-5Vdc	0	1	0	1	1	0	1	0
0	1	1	1	1	0	0	0	0

International Journal of Advance Research in Science and Engineering
Vol. No.5, Issue No. 11, November 2016
www.ijarse.com
IJARSE
ISSN (O) 2319 - 8354
ISSN (P) 2319 - 8346

III. MODULATION SCHEMES

Different PWM techniques are used to produce the switching pulses for the single phase inverter. PWM techniques are used to control the frequency and to reduce the harmonics. A simple method to generate the PWM pulse is to compare reference wave which is usually a sine wave with a carrier signal which is a saw tooth or triangular signal. As shown in Fig 3-

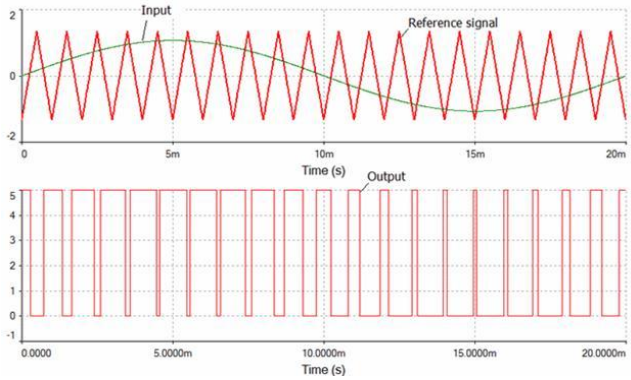

Fig 3: *Generation of PWM pulse*

The advantage of PWM is that there is very low power loss in the switching device. When a switch is off there is no current n it and when it is on and power is transferred to the load there is negligible voltage drop. Here the modulation indicer are same for all the methods. The amplitude modulation index is 0.9 and the frequency modulation index is 200.

The Pulse width modulation methods used in this paper are In-phase disposition level shift PWM method, Anti-phase disposition level shift PWM method, Carrier overlap PWM method, Variable frequency PWM method.

3.1 IN-PHASE DISPOSITION LEVEL SHIFT PWM (IPD-LSPWM) METHOD

In this method the carrier signals are level shifted. Also here as carrier signals are in phase across all the bands, the harmonic energy is concentrated at the carrier frequency. The amplitude of the carrier signal is 1V and frequency is 10 kHz. And it is compared to a reference sine wave.

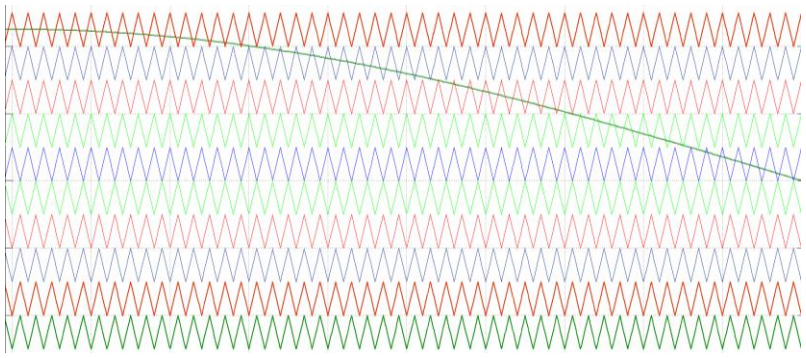

Fig 4: *Reference and carrier wave For IPD-LSPWM*

IJARSE
ISSN (O) 2319 - 8354
ISSN (P) 2319 - 8346

3.2 ANTI-PHASE DISPOSITION LEVEL SHIT PWM (APD-LSPWM) METHOD

In this method the carrier signals are out of phase with each other by 180^0. The amplitude and frequency is same.

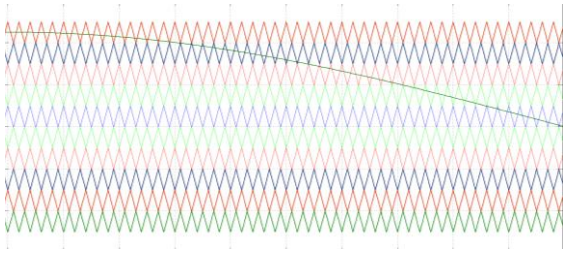

Fig 5: *Reference and carrier wave For APD-LSPWM*

3.3 CARRIER OVERLAP PWM (COPWM) METHOD

The carrier signals are level shifted and they are in phase with each other and also they overlap one another. Carrier signals are compared to a sine wave.

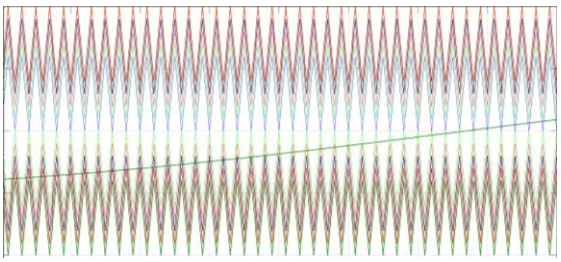

Fig 6: *Reference and carrier wave for COPWM*

3.4 VARIABLE FREQUENCY PWM (VF-PWM) METHOD

Carries signals are level shifted and of same amplitude. But they have different frequencies. The lowermost carrier wave has frequency equal to 10kHz followed by 8 kHz 6kHz 4kHz 2kHz. Higher the frequency higher will be the pulses.

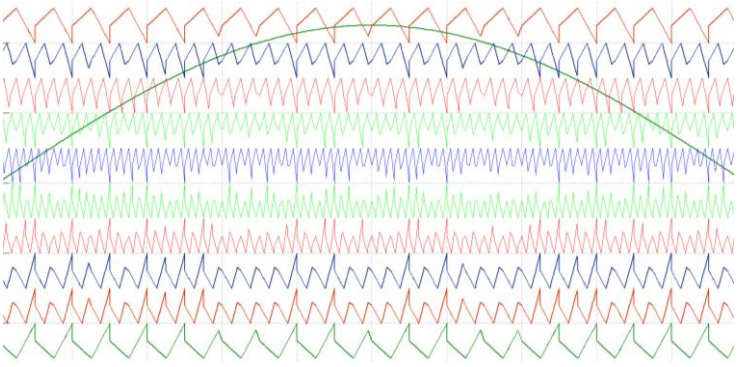

Fig 7: *Reference and carrier wave for COPWM*

International Journal of Advance Research in Science and Engineering
Vol. No.5, Issue No. 11, November 2016
www.ijarse.com
IJARSE
ISSN (O) 2319 - 8354
ISSN (P) 2319 - 8346

IV. SIMULATION CIRCUITS

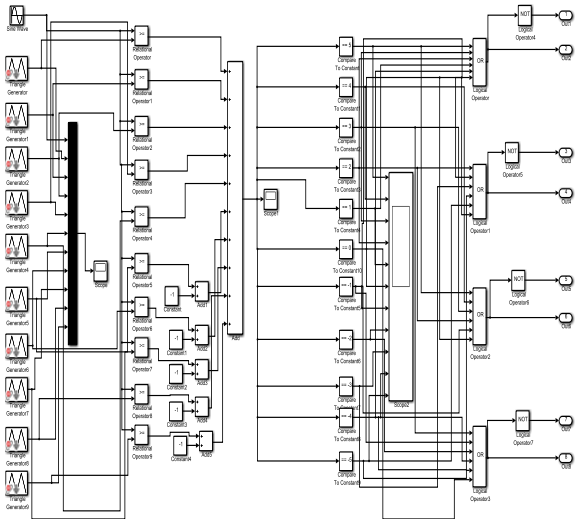

Fig 8*: Simulation circuit to generate the swithcing pulse*

Fig 8 shows how the gate pulse for the eight swithches in inverter are produced. Ten trianglepulse generators are used to produce triangle waves in positive and negative halves. A sine wave generator is used to produce a sine wave and then these waves are compared with the help of relational operator.

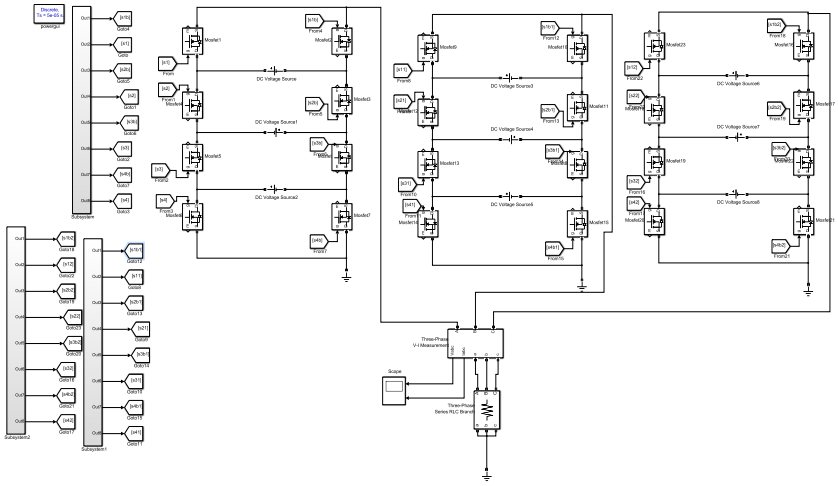

Fig 9*: 3 phase inverter simulation circuit to produce 11 level output waveform*

In order to obtain a three phase inverter the sine wave is phase shifted by 120^0.

V. SIMULATION RESULTS

Various PWM techniques are applied to the proposed 11 level inverter topology. Their output voltage and FFT analysis is given as follows:

International Journal of Advance Research in Science and Engineering
Vol. No.5, Issue No. 11, November 2016
www.ijarse.com
IJARSE
ISSN (O) 2319 - 8354
ISSN (P) 2319 - 8346

5.1 In-Phase disposition PWM method

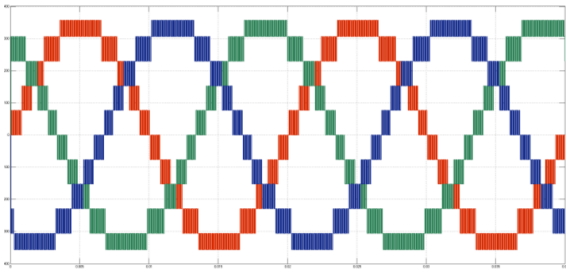

***Fig 10**: Output voltage waveform for three phase 11 level inverter using IPD-LSPWM*

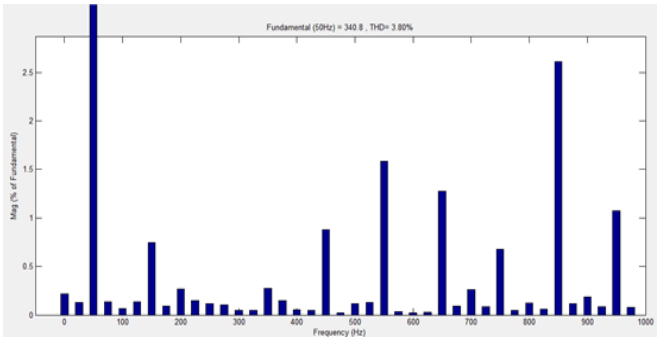

Fig 11:*FFT analysis of harmonics for IPD-LSPWM*

5.2 Anti-Phase disposition PWM method

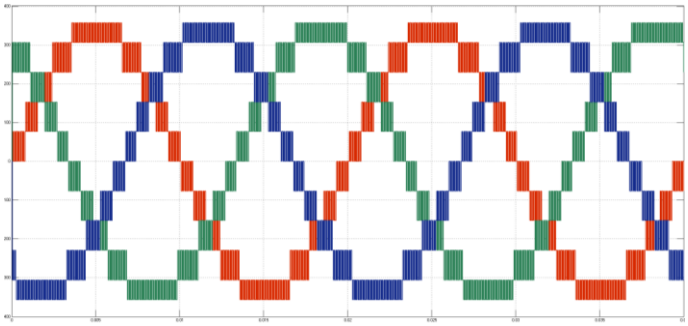

Fig 12*: Output voltage waveform for three phase 11 level inverter using APD-LSPWM*

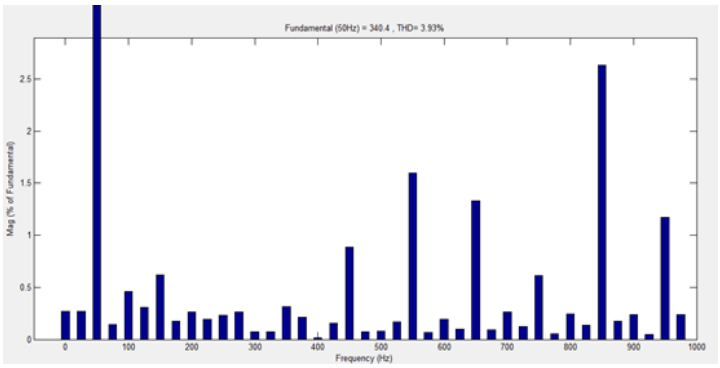

Fig 13: *FFT analysis of harmonics for APD-LSPWM*

International Journal of Advance Research in Science and Engineering
Vol. No.5, Issue No. 11, November 2016
www.ijarse.com
IJARSE
ISSN (O) 2319 - 8354
ISSN (P) 2319 - 8346

5.3 Carrier overlap PWM method

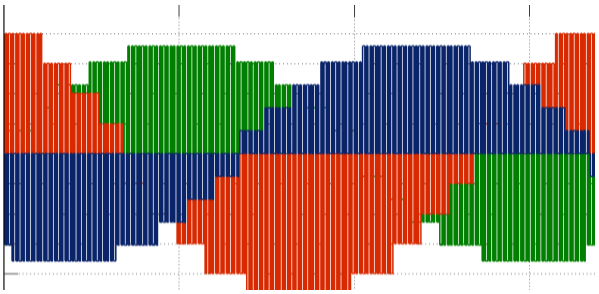

Fig 14: *Output voltage waveform for three phase 11 level inverter using COPWM*

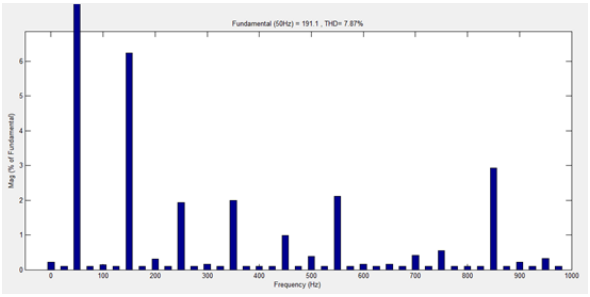

Fig 15: *FFT analysis of harmonics for COPWM*

5.4 Variable frequency PWM method

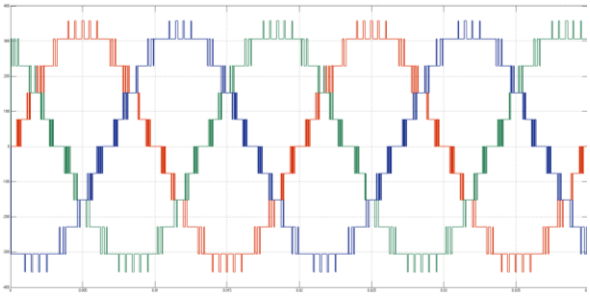

Fig 16 : *Output voltage waveform for three phase 11 level inverter using VFPWM*

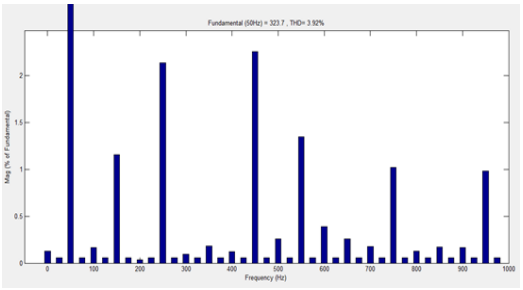

Fig 17: *FFT analysis of harmonics for COPWM*

IJARSE
ISSN (O) 2319 - 8354
ISSN (P) 2319 - 8346

VI. CONCLUSION

1. Three Phase 11 level inverter topology with less number of switches is proposed and simulated. Various PWM methods are analysed and compared.
2. From simulation results and THD analysis it is found that In-phase level shift PWM method provides minimum 3.80% in the output voltage. Therefore this will be the best PWM technique for inverter switching.

Table 2: *THD using PWM methods*

Method	Total Harmonic Distortion(Calculated)
IPD-LSPWM	3.80%
APD-LSPWM	3.93%
COPWM	7.87%
VFPWM	3.92%

REFERENCES

[1] Rahul Nair; MahalaxmiR ;Dr.SindhuKampatty K.C.: Performance of 11 level inverter with reduced no. of switches usingdiffertent PWM techniques,2015IEEE International Conference on Technological Advancements in Power & Energy.

[2]Rodriguez J., Lai J.S., PengF.Z.'Multilevel inverters: A survey of topologies, controls, and applications'. IEEE Trans. Ind. Electron., vo1.49,no. 4, pp. 724-738, Aug. 2002.

[3] Malinowski, M.; Gopakumar, K.; Rodriguez, J.; Perez, M.A; , "A Survey on Cascaded Multilevel Inverters," Industrial Electronics, IEEE Transactions on , vo1.57, no.7, pp.2197-2206, July 2010.

[4] Balamuruganc.R., Natarajan S.P., Vidhya V.' A New Modified Hybrid Hbridge Multilevel Inverter using less Number of Switches'. International Conference on Computation of Power, Energy, Information and Communication (ICCPEIC), 2013, pp 1-6.

[5] Mohamed AS, Norman Mariun, NasriSulaiman, MArnran M. Radzi :"A New Cascaded Multilevel Inverter Topology with Minimum Number of Conducting Switches," IEEE Innovative Smart Grid Technologies-Asia (ISGT ASIA) 2014.

[6] Khomfoi S., Praisuwanna N., Tolbert L.M. :"A Hybrid Cascaded Multilevel Inverter Application for Renewable Energy Resources Including a Reconfiguration Technique," Electrical Engineering and Computer Science, The University of Tennessee, USA

IJARSE
ISSN (O) 2319 - 8354
ISSN (P) 2319 - 8346

[7] Salodkar P., Sandeep N., Kulkarni P.S., Ajaykumar R.Y.:'A Comparison of Seven-Level Inverter Topologies for Multilevel DC-AC Power Conversion'. IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES), 2014.

[8] Beigi L.M.A., Azli N.A., Khosravi F., Najafi E., Kaybhosravi A: 'A New Multilevel Inverter Topology with less Power Switches', International Conference on Power and Energy, 2012, IEEE , 2-5 December 2012.

[9] Vadhiraj S., NarayanaSwamy K., Divakar B.P. ;, "Generic SPWM Technique for Multilevel Inverter," Electrical and Electronics Dept, REVA Institute of Technology and Management, Bangalore, India.

[10] Hyosung Kim, Seung-Ki Sui, "Analysis on Output LC Filters for PWM Inverters", Power Electronics and Motion Control Conference, 17-20 May2009. IPEMC, 2009. IEEE 6th International, Pp. 384 - 389.