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FRC BASED IPC STRATAGEM FOR MLI-DSTATCOM COMPENSATING UNBALANCES IN POWER DISTRIBUTION NETWORK

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ABSTRACT

Distribution Static synchronous Compensators (DSTATCOMs) are tried a good approach to compensate reactive current in distribution network. With positive-sequence element, negative-sequence and 0 sequence element of unbalanced load current detected severally, selective reactive current compensation with individual section management strategy are often accomplished. to enhance the steady compensate performance while not sacrificing its dynamic performance, quick repetitive managementler primarily based compound current control methodology for cascaded DSTATCOM compensating unbalanced load is planned during this paper. DC-link voltage leveling management methodology is additionally introduced to take care of the balance of DC-link voltages of H-inverters. Finally, simulation and experimental results from H-bridge cascaded DSTATCOM verify the feasibleness and potency of the planned methodology.

Keywords: Cascaded DSTATCOM; Unbalanced Load; Fast Repetitive Controller; Individual Phase Control

I. INTRODUCTION

As new generation reactive power compensation instrumentation, DSTATCOM injects governable current at the purpose of common coupling (PCC) in order that reactive power compensation, harmonic current suppression, load leveling, and PCC voltage stabilization are often achieved. H-bridge cascaded construction electrical converter based mostly DSTATCOM is finding exaggerated attention in medium voltage and dynamic applications thanks to its benefits.

The unbalanced load operation may be a common drawback that STATCOM trot out. For transformer-less star-configured cascaded DSTATCOM, since the DC-link capacitors of the H-bridges converters square measure split and isolated, the active power can't be changed between the section legs. Therefore, it's a challenge for the present management loop to search out the optimum reference voltages for following reference current and

maintaining zero average power at the same time below unbalanced conditions. A zero-sequence voltage which might counteract the active power caused by the negative-sequence current is sometimes injected into the overall reference voltage to create the STATCOM work steady. However, acquisition of the zero-sequence voltage reference may be a complicated calculation method, meanwhile, the STATCOM wants increase its DC-link voltage output thanks to the zero-sequence voltage element. For three-phase four-wire system, unbalanced load compensation are often simply achieved below individual section operation, besides, DC-link voltage leveling isn't any longer a retardant thanks to the neutral line will give conductivity path for active power flowing into or out of per section leg.

In this paper, individual section management strategy for 3 sections four-wire cascaded DSTATCOM by selection compensating unbalanced load is planned. DC-link voltage leveling management technique geared toward maintaining the balance of DC-link voltages of H-inverters is additionally introduced. To enhance compensation accuracy while not sacrificing dynamic response, quick repetitive management (FREP) was adopted for the look of double-loop management strategy supported proportional integral (PI) inner loop and FREP outer loop. Finally, Matlab/simulink model of three-phase four-wire DSTATCOM was made with experiments dispensed on DSTATCOM industrial paradigm, each simulation and experimental results show the validity and practicability of all analysis.

II. CASCADED DSTATCOM SYSTEM

The scheme of cascaded DSTATCOM considered in this paper is the three-phase four-wire configure as shown in Fig.1.

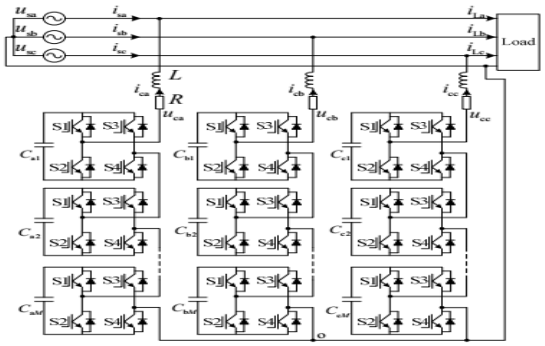

Fig. 1. Topology of Three-Phase Four-Wire Cascaded Dstatcom.

The electrical converter of DSTATCOM consists of many H-bridge power electrical converter cells connected asynchronous per section. Every electrical converter cell incorporates a floating DC-link capacitance. DSTATCOM is connected to the purpose of Common Coupling (PCC) through Associate in nursing ac inductance L (with identical resistance R) that makes a necessary contribution to filtering out change ripples. usi (i=a,b,c) is grid voltage, iLi is load current, whereas uci and ici square measure output voltage and output current of DSTATCOM, severally.

Since every section of the DSTATCOM is freelance within the three-phase four-wire stellate system, the management objects are often deduced in identical single-phase circuit merely. The single-phase equivalent circuit attentively paid to the A-phase of the DSTATCOM is shown in Fig.2.

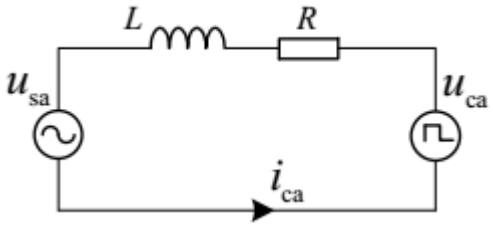

Fig. 2. Single-Phase Equivalent Circuit of The DSTATCOM

From Fig.2, the single-phase time-domain version of DSTATCOM is written in (1). Then s-domain switch feature of the controllable voltage source u_{ci} to the grid side modern i_{ci} may be derived as (2).

III. DESIGN OF INDIVIDUAL PHASE CONTROL STRATEGY

3.1 Unbalanced Reactive Current Detection Method

In three-phase four-wire system, unbalanced load current may well be rotten to positive, negative and nil sequence elements. While not harmonics thought-about, the steady-state load current may be written as in (3).

$$\begin{Bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{Bmatrix} = I_P \begin{Bmatrix} \sin(\omega t+\varphi_P) \\ \sin(\omega t+\varphi_P-\frac{2\pi}{3}) \\ \sin(\omega t+\varphi_P+\frac{2\pi}{3}) \end{Bmatrix} + I_N \begin{Bmatrix} \sin(\omega t+\varphi_N) \\ \sin(\omega t+\varphi_N+\frac{2\pi}{3}) \\ \sin(\omega t+\varphi_N-\frac{2\pi}{3}) \end{Bmatrix} + I_0 \begin{Bmatrix} \sin(\omega t+\varphi_0) \\ \sin(\omega t+\varphi_0) \\ \sin(\omega t+\varphi_0) \end{Bmatrix} \quad (3)$$

where ω is grid frequency, IP, IN and I0 are amplitudes of the three components, with the initial phase angle of φP, φN and φ0, respectively.

By applying synchronous rotating transformation as in (4), the load current in positive-sequence and negative-sequence synchronous coordinate can be written as in (5) and (6), respectively. Subscripts "+" and "-" respectively represent for the positive-sequence and the negative-sequence synchronous coordinates.

$$T_{dq} = \frac{2}{3}\begin{bmatrix} \sin\theta & \sin(\theta-2\pi/3) & \sin(\theta+2\pi/3) \\ \cos\theta & \cos(\theta-2\pi/3) & \cos(\theta+2\pi/3) \end{bmatrix} \quad (4)$$

$$\begin{Bmatrix} i_{Ld+} \\ i_{Lq+} \end{Bmatrix} = I_P \begin{Bmatrix} \cos\varphi_P \\ \sin\varphi_P \end{Bmatrix} + I_N \begin{Bmatrix} -\cos(2\omega t+\varphi_N) \\ \sin(2\omega t+\varphi_N) \end{Bmatrix} \quad (5)$$

$$\begin{Bmatrix} i_{Ld-} \\ i_{Lq-} \end{Bmatrix} = I_P \begin{Bmatrix} \cos(2\omega t+\varphi_P) \\ \sin(2\omega t+\varphi_P) \end{Bmatrix} + I_N \begin{Bmatrix} -\cos\varphi_N \\ \sin\varphi_N \end{Bmatrix} \quad (6)$$

It are often finished that in positive-sequence synchronous coordinate, the positive-sequence element of load current is rotten into a continuing active element and a continuing reactive one in steady state, with the negative-sequence element of double grid frequency. Whereas in negative sequence synchronous coordinate, the result's precisely the opposite.

Then the reactive current detection technique supported positive/negative sequence synchronous rotating rework is represented in Fig.3, wherever MAF is moving average filter liable for sweeping away double grid frequency harmonics in synchronous coordinates, Tdq and Tdq -1 area unit synchronous rotating transformation and its

inverse transformation, severally. Iref,iP and irefi,N area unit positive sequence and negative-sequence references of unbalanced load current, whereas iref0 is zero-sequence reference no heritable directly in stationary coordinate.

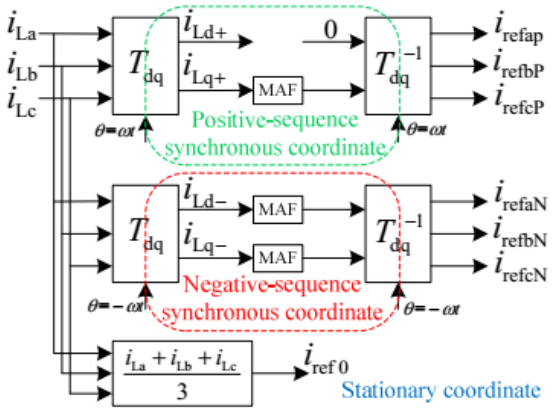

Fig. 3. Block Diagram of Detection Method for Unbalanced Load.

With positive-sequence element, negative-sequence and zero-sequence element detected severally, selective reactive current compensation mode is complete. To compensate negative-sequence and zero-sequence element solely (unbalanced compensate mode), the present reference of i-phase irefi (i=a,b,c) is given as (7), whereas the present reference for full compensate mode(with positive-sequence, negative sequence and zero-sequence element totally compensated) is represented in (8).

$$i_{refi}=i_{refiN}+i_{ref0} \qquad (7)$$

$$i_{refi}=i_{refiP}+i_{refiN}+i_{ref0} \qquad (8)$$

3.2 Fast Repetitive Controller based Compound Control

Generally, this reference in stationary frame could be a curved element, and it's of little question that single proportional integral (PI) controller cannot track it with zero steady-state error. Repetitive controller relies on the interior model principle which may introduce infinitely open amplification at periodic signal's first harmonic and its harmonics, so will track periodic signal with zero steady-state error.

The diagram of ancient repetitive controller (REP) is delineated as Fig.4, where R(z), E(z), d(z) and Y(z) square measure the reference signal, error signal, outer disturbance and feedback signal, severally. GP(z) is that the management plant, N is that the samples variety during a basic amount.

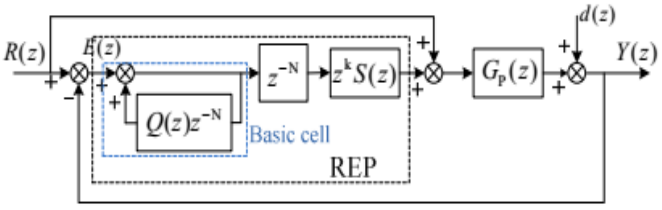

Fig. 4. Block Diagram of Traditional Repetitive Control.

In ancient repetitive controller, thanks to the delay half within the forward channel, the samples variety to refresh the REP internal model is N, specifically the error signal examined during this amount will solely be utilized in consecutive amount, and an inherent basic amount delay is exist. In fact, the fundamental cell of REP could be a regeneration of a delay of N sampling periods wherever N=tr/ts, tr being {the amount the amount} of the periodic signal to be tracked or rejected and ts the sampling period.

To improve the dynamic performance, quick repetitive controller (FREP) has been improved as in Fig.5. Completely different from REP, FREP relies on a cell that consists of a feedback of a delay of N/2 sampling periods.

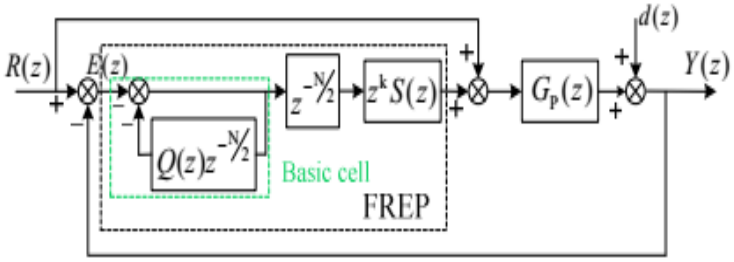

Fig. 5. Block Diagram of Fast Repetitive Control.

Obviously, the samples variety to refresh the FREP internal model is N/2, particularly the error signal examined during this [*fr1] amount are often employed in consecutive [*fr1] amount, and in consequence inherent delay of FREP is simply [*fr1] a elementary amount, therefore FREP is of a much better dynamic performance that that of ancient REP. Fig.6 shows the signal plot of REP and FREP basic cells. It are often tested that the fundamental cell of REP has poles at fundamental and its all harmonic frequencies, whereas the cell has poles at fundamental and its odd harmonic frequencies.

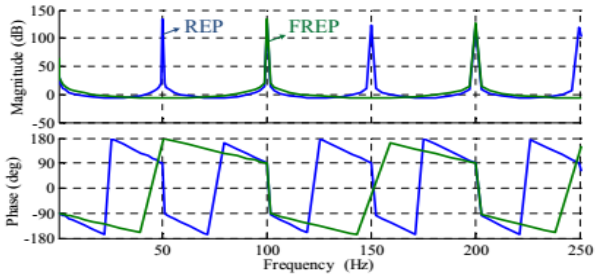

Fig. 6. Bode Plot of REP and FREP Basic Cells.

Then compound current control strategy consists of inner PI control loop and outer fast repetitive control loop is introduced as in Fig.7.

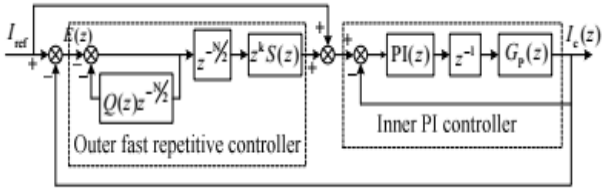

Fig. 7. Diagram of frep Based Compound Current Control Strategy.

For the inner PI management loop, GP(z) is z-domain transfer operate of DSTATCOM management plant, PI(z) is PI controller that is meant supported zero-poles cancellation methodology so discretized into z-domain consistent with the Tustin approximation methodology, z-1 is that the inherent unit delay of the digital implementation. The open-loop transfer operate of the inner PI management loop are often represented as

$$G_{\text{Plo}}(z) = z^{-1} PI(z) G_{\text{p}}(z) \qquad (9)$$

Then the close-loop transfer function of the inner loop is

$$G_{\text{PIc}}(z) = \frac{G_{\text{Plo}}(z)}{1 + G_{\text{Plo}}(z)} \qquad (10)$$

The outer FREP management loop consists with internal model, 0.5 basic amount delay part (z-N/2) and corrector (zkS(z)), wherever Q(z) is attenuation filter that is typically a continuing smaller than unit, S(z) may be a second order digital filter wont to depress the gain of GPIc(z) in high frequency vary, whereas the k-beat leading part (zk) will compensate the part lag of the inner PI management loop. Fig.8 shows the prognosticate plot of GPIc(z) and zkS(z)GPIc(z). It will be seen in Fig.8 that the part lag of GPIc(z) was reduced from ten degree to close to zero degree at 50Hz and from twenty two degree to close to zero degree at 100Hz. Hence, compensation exactness will be greatly promoted because of abundant less part lag.

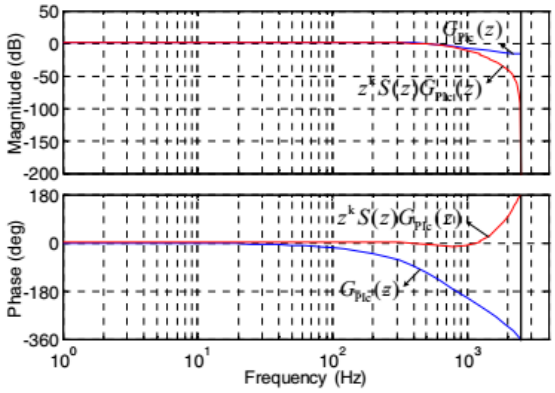

Fig. 8. Bode Plot of *G*pic(Z) and Z^ks(Z)*G*pic(Z).

3.3 DC-link Voltage Balancing Control

The main task of the DC-link voltage reconciliation management technique is to stay DC-link voltages at a needed level that is of nice importance for the stable operation of DSTATCOM. It are often classified into total DC-link voltage reconciliation management and in-phase DC-link voltage reconciliation management.

To maintain the full DC-link voltage at the reference worth, the DC-link condenser has to exchange a particular quantity of active power with the grid, that is proportional to the distinction between the particular and reference voltages. In total DC-link voltage management as in Fig.9, the active power is generated by chase active current reference synchronous with grid voltage. udcref is DC-link voltage reference, M is cascade variety and idcrefi is that the active current reference.

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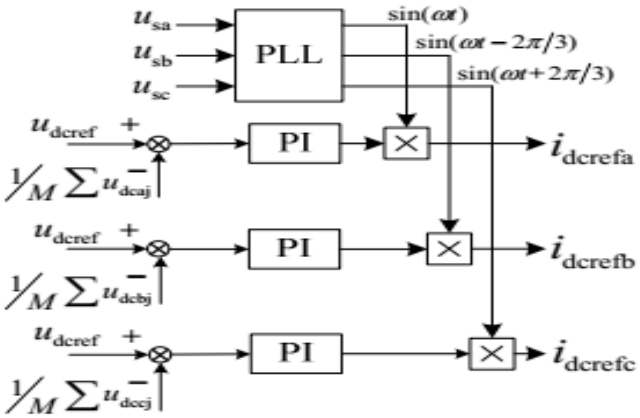

Fig. 9. Block Diagram of Total DC-Link Voltage Balancing Control.

In-phase DC-link voltage reconciliation management is additionally indispensable as a result of internal losses of H-bridges don't seem to be identical, DC-link voltage of every H-bridge are simply unbalanced while not management. This reconciliation technique for M Hbridges in every explicit part relies on the insertion of further voltage elements ubanij (i=a,b,c; j=1,2,…M) within the output voltages of every H-bridge. and also the voltage part is in part or in anti-phase with DSTATCOM output current.

At last, the individual part management strategy is delineate in Fig.10, where, irefi and idcrefi square measure severally reactive current reference and active current reference mentioned antecedently. The output of the individual part management urefij is that the DSTATCOM output voltage reference for corresponding H-bridge electrical converter, that is that the signal introduced to the PWM modulator.

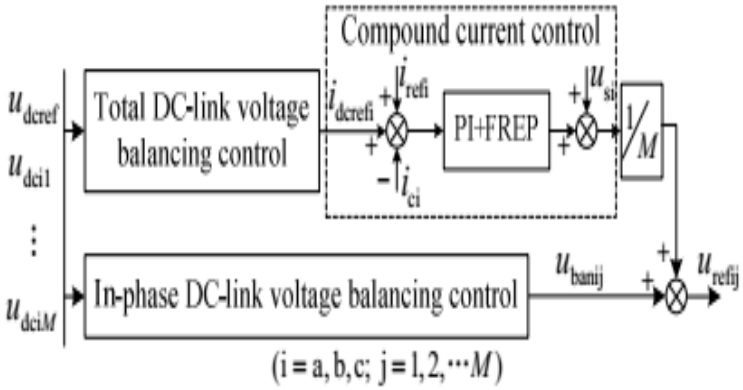

Fig. 10. Block Diagram of Individual Phase Control for CASCADED Dstatcom

IV. SIMULATION RESULTS

To verify practicableness and potency of the planned methodology, simulations below MATLAB/Simulink atmosphere and experiments on cascaded DSTATCOM example are meted out. The unbalanced load is grooved by balanced resistive load and unbalanced inductive load. Table I shows main parameters of cascaded DSTATCOM system. Carrier section shift curving pulse breadth modulation (CPS-SPWM) is used for the drive of H-bridge IGBTs

Table I. Main Parameters of Cascaded Dstatcom System

Line-to-line voltage	380V
Grid frequency	50Hz
AC inductor	2mH
DC-link capacitor	5mF
DC-link voltage	150V
Cascade number	3
Sampling frequency	10.0kHz
SPWM carrier frequency	4.0kHz

Fig.11 Shows Current Tracking Behavior For Sinusoidal Reference Step with REP and FREP Controller Playing The Role of Outer Controller, Respectively.

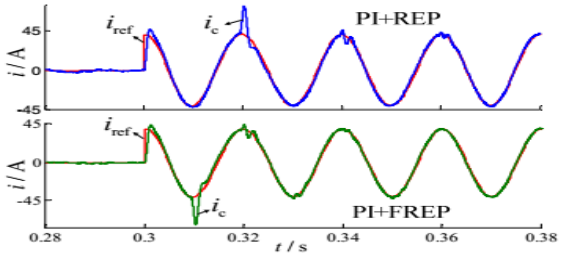

Fig. 11. Current tracking behavior for sinusoidal reference step with traditional and fast repetitive control

Where, iref is current reference, and ic is DSTATCOM output current. It is seen thet the reference experiences a transient modification at the time t=0.3s, and REP doesn't work till t=0.32s, whereas FREP starts to figure at regarding t=0.31s, particularly the time interval of FREP is simply [*fr1] the time of REP, that is per the theoretical analysis.

Fig.12 shows the simulation results of DSTATCOM compensating for reactive load, and Fig.13 shows grid voltage and grid current. iL, ic and is square measure load current, DSTATCOM output current and grid current, severally, udc is DC-link voltages of the individual H-bridges in phase-A.

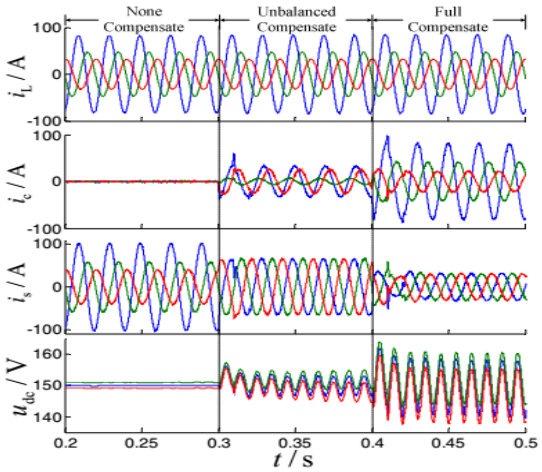

Fig. 12. Simulation Results of DSTATCOM Compensating Unbalanced Load.

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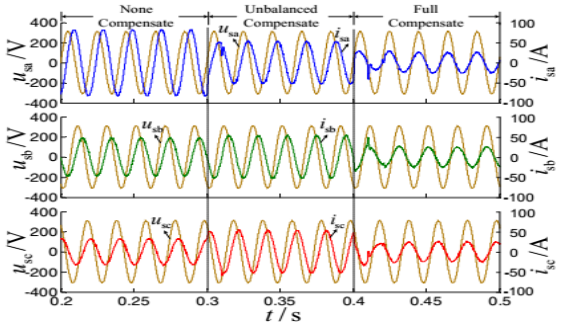

Fig. 13. Grid Voltage and Grid Current of Each Phase

Three completely different compensate modes of DSTATCOM are simulated. 1).During the interval from zero.2s to 0.3s, DSTATCOM doesn't compensate any reactive current once the output current is barely a touch active current changed with grid to keep up the equalization of DC-link voltages, and therefore the grid current is unbalanced, or so capable load current. 2).From 0.3s to 0.4s, DSTATCOM operates within the mode of compensating negative-sequence and zero-sequence reactive current (unbalance compensate mode). This point grid current tends to be balanced with negative-sequence and 0 sequence current injected to the load from DSTATCOM, however the ability issue is extremely low from the visible part distinction between grid voltage and grid current in every part, which may be seen in Fig.12. 3).At 0.4s, DSTATCOM turns into full compensate mode with 3 reactive current parts absolutely paid. It's determined that grid voltage and current stay in part throughout the steady state amount below full compensate mode. This means that the ability issue of the grid is getting ready to unit one, and therefore solely active power is drawn from the supply.

Besides, the DC-link voltages is well balanced throughout the total simulation, the ripple of double grid frequency within the DC-link voltage is usually because of the reactive current flow between DSTATCOM with grid. From the steady-state performance of DSTATCOM below completely different compensate mode shown in Table II, it will draw a conclusion that the planned strategy will compensate unbalanced load excellently with high equalization performance yet as low total harmonic distortion (THD) of grid current.

Table II. Steady-State Performance Under Different Modes

Compensate Mode	Grid Current		
	Current	*RMS* (A)	*THD* (%)
None Compensate mode	i_{sa}	102.8	0.31
	i_{sb}	58.9	0.46
	i_{sc}	40.3	0.66
Unbalanced Compensate mode	i_{sa}	66.0	0.66
	i_{sb}	66.3	0.50
	i_{sc}	65.8	0.60
Full Compensate mode	i_{sa}	32.2	1.31
	i_{sb}	31.3	0.95
	i_{sc}	31.1	0.82

V. CONCLUSION

This paper proposes individual section management strategy consists of quick repetitive managementler based mostly compound current management and DC-link voltage equalization control for three-phase four-wire cascaded DSTATCOM. With positive-sequence part, negative-sequence and zero-sequence part of unbalanced load current detected severally, the selective reactive current compensation with individual section management is complete, quick repetitive controller will improve the steady compensate performance while not sacrificing dynamic performance. Meanwhile, DC-link voltage equalization management will maintain the equalization of every DC-link voltage that is precondition for stable operation of cascaded DSTATCOM.

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