International Journal of Advance Research in Science and Engineering
Vol. No. 5, Special Issue No. 01 , May 2016
www.ijarse.com
IJARSE
ISSN 2319 - 8354

POWER QUALITY ENHANCEMENT USING BRIDGELESS CONVERTER BASED ON MULTIPLE OUTPUT SMPS

Mr. Gajkumar R. Kavathekar[1], Mr. Kiran Nathgosavi[2], Mr. Suhas Sutar[3]

[1]*Electrical engineering, ADCET, Ashta,(India)*

[2]*Electrical engineering, RIT, Islampur, (India)*

[3]*Electrical engineering, VTC, Miraj, (India)kll*

ABSTRACT

This paper introduces a design, analysis, simulation and improvement of power factor (PF)multiple output Switched Mode Power Supply (SMPS) using a bridgeless non buck-boost DC-DC converter is used as the first stage. The first stage buck-boost converter is designed in Discontinuous Conduction Mode(DCM) for inherent power factor correction (PFC). Comparing with conventional topologies the proposed topology reduces conduction losses and improves power quality. Both simulation and experimental results demonstrate the improved performance of the proposed SMPS.

Keywords: DC-DC Converter, discontinuous conduction mode (DCM), improved power quality, PFC, SMPS, THD.

I. INTRODUCTION

Switched mode power supply (SMPS) are extensively usedin various application such as machine tools, industrials securities, support supplies with PLCs and personal computers. Switched mode power supplies (SMPS) commonly employed to powering up the different parts in personal computer (PC) by generatingmultiple Dc voltages from single phase AC supply. Multiple outputs of SMPS is mainly applicable for PCs to power up USB, Mouse, monitor and many digital and analog circuits. But SMPS operation usually suffers from low power factor at theinput AC mains. The reason is commonly used diode bridge rectifier front end of the SMPS.This topology leads to poor power quality of the system mainly high THD (Total harmonic distortion), low power factor, poor voltage regulation, high conduction losses & high crest factor for AC input current.[1]Due to increasing awareness towards power quality many manufactures related to power supply implemented power factor correction circuit at utility interface side so that they can maintain power quality standards as stated by IEEE 519 & IEC 61000 [2]-[3]. This become serious problem when large numbers of PCs are connected at common point, due effect like overloading of neutral conductor, noise, voltage distortion & de-rating of transformer [4]. Bridgeless powerfactor correction converter at the front end of the SMPS is expected to draw a sinusoidal input current at high powerfactor. Improvement in power quality also results in better efficiency. This paper deals with the development of bridgeless rectifier based dual output SMPS specially designed for low powerapplications. In proposed two stage multiple output switched mode power supply

bridgeless buck –boost converter is operate for both positive as well as negative cycle as a first stage. a half bridge inverter connected to the high frequency transformer is usedfor isolation and for getting multiple outputs.

II. CIRCUIT CONFIGURATION AND ANALYSIS

The system configuration of the proposed multiple-output SMPS is shown in Fig. 1. In this configuration it involves two buck boost converter, PFC, voltage source inverter,high frequency transformer, high frequency switches, and diodes. To eliminate the high frequency ripples single-phase ac supply is fed to two buck–boost converters through an inductor–capacitor (Lin–Cin)filter. Upper buck-boost converter works on the positive half cycle of the input ac supply. Similarly, lower buck-boost converter works on the negative half cycle of the input ac supply. During the positive half cycle of the ac supply consist of one high-frequency switch Sp, inductor Lp, and two diodes Dp1 and Dp2. During negative half cycle consists of one high-frequency switch Sn, inductor Ln andtwodiodes Dn1 and Dn2.[1].

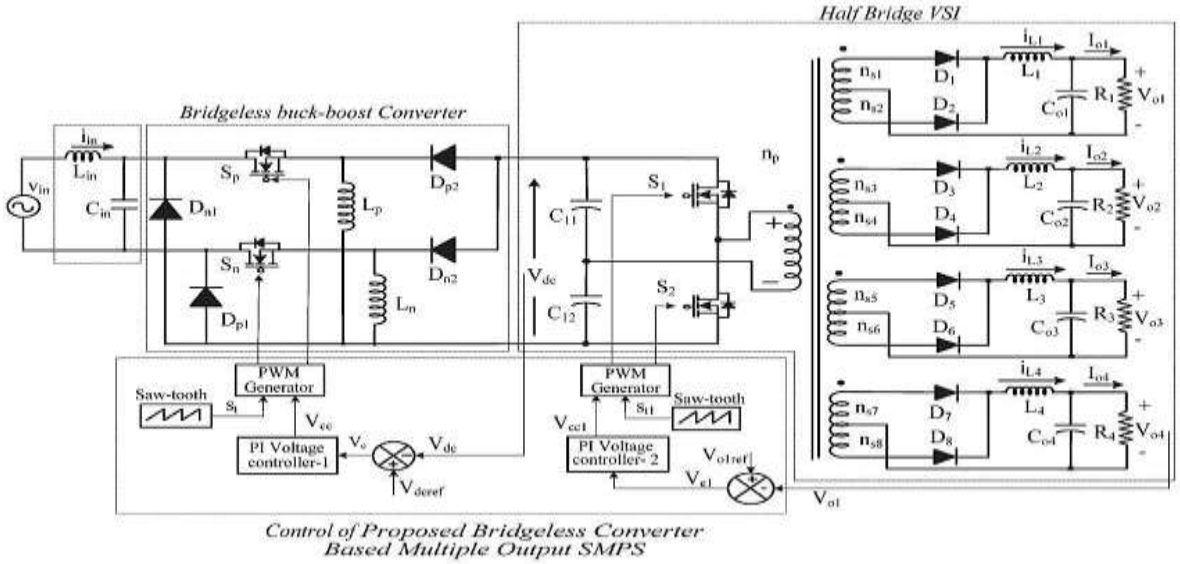

Fig 1-Circuit Configuration Of Proposed Multiple Output Switched Mode Power

Bothinductors Lp and Ln of buck–boost converters are designed in such way that they should insure DCM operation of converter to obtain inherent PFC at the input ac mains.Now in the operation of voltage source inverter capacitor placed at input side of half bridge VSI acts as filter for DC output of buck-boost converter.The output dc voltage of the buck–boost converter is regulated by using closed-loop control.This regulated output voltage is feed to the voltage source inverter for obtaining multiple outputs.The half-bridge VSI consists of two input capacitors C11 and C12,twohigh-frequency switches S1 and S2,andonemultipleoutput high-frequency transformer (HFT).The HFT is consist of one primary winding and four secondary windings which are connected in center-tapped configuration to reduce the losses[1].inductor L1,L2,L3 L4 and capacitor C01,C02,C03,C04 are used to limit the ripples present in voltage and current. Highest output voltage is sensed for controlling purpose of voltage source inverter.

International Journal of Advance Research in Science and Engineering
Vol. No. 5, Special Issue No. 01 , May 2016
www.ijarse.com
IJARSE
ISSN 2319 - 8354

III. WORKING OF BASED BRIDGELESS-CONVERTER MULTIPLEOUTPUT SMPS

This designed system model consists of two back to back buck-boost converters, half bridge voltage source inverter, and multiple output high frequency transformers at the load end. The buck boost converter is appropriately controlled for obtaining high power factor and low input current THD. The operation of converter for one switching cycle is given as follows,

3.1 Working of Buck–Boost Converter

This bridgeless buck-boost converter is consists of the upper and lower switch which are conducted for positive and negative cycle input ac voltage respectively. The operation of the upper buck–boost converter in DCM during the positive half cycle of the ac input voltage is shown in Fig. 3.

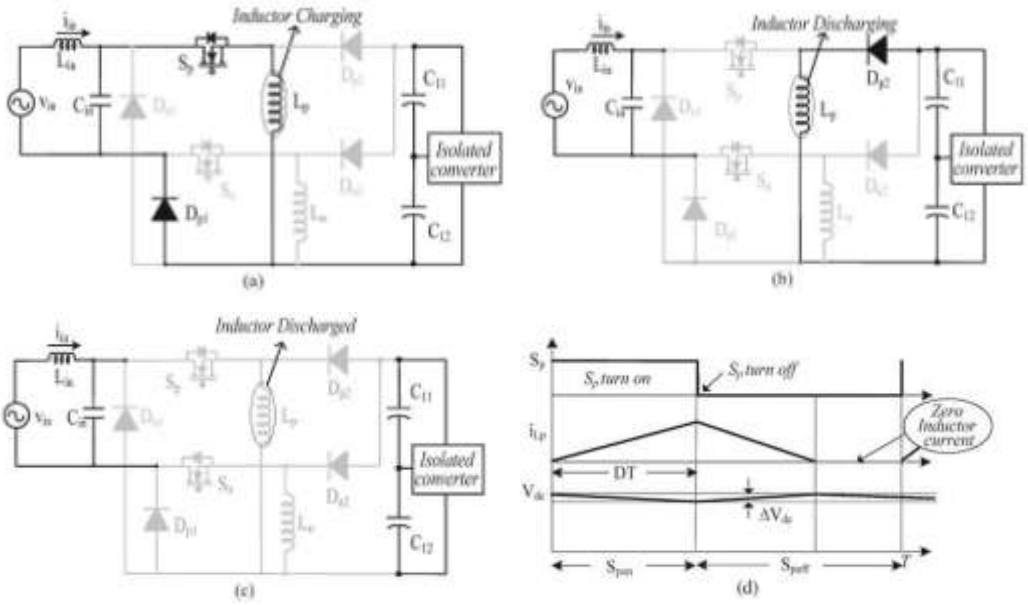

Fig.3. Operating modes for under (a) upper switch Sp is on, (b) upper switch Sp is off, (c) bothswitch and diodeare off,and (d)waveforms in one switching cycle.

When we deal with DCM operation it should be takes place in three stages .In first stage when pulse given to the upper switch Sp, switch Sp is on, then inductorLp associated with it start for storing energy from input ac supply, during this stage inductor current increases from minimum (zero) value to maximum value, as shown in fig. 3(a).Diode Dp1 completes the current flow path in the input side. In second stage switchSp is get turned off, and inductorLp starts for discharging through capacitor so that inductor current decreases from maximum value to zero,as shown in fig. 3(b). In the last stage of one switching cycle, neither diode nor switches are conduct so that inductor current become zero during this stage. Zero current of inductor itself ensure the DCM operation, as shown in fig. 3(c). Fig. 3(d) shows the waveforms for one complete pulse width modulation (PWM) switching cycle. Like this lower buck boost converter is operated for the negative half cycle.

3.2 Working Of Half Bridge Voltage Source Inverter

The controlled output dc voltage of the dual buck–boost converter is fed to the half-bridge VSI as input for high-frequency isolation, for voltage scaling, and for obtaining multiple dc output voltages. Working of half bridge VSI for one switching cycle is divided in to four sub stages. The second andfourth stages are similar and occur twice in each switching cycle. In first stage out of two switches when upper switch S1 is tuned on it starts for conducting input current through primary winding of HFT to the lower input capacitor C12.During this diodes D1, D3, D5, D7 on the secondary side are forward biased and the current will flow through respective inductor so that inductor current increases while output capacitor discharging through the load.In second stage of operation both switches are turned off and all the diodes on secondary side are comes in freewheeling mode. Due to this inductor start for deceases .In third stage lower switch is turned on and current will flows through upper capacitor and primary winding of the high frequency transformer. The diode son secondary side D2, D4, D6, D8 is conducting due to which inductor current start for storing the energy. Switch is turned off when energy in inductor becomes maximum. In fourth stage all diodes on secondary are in freewheeling mode and same operation is repeated as given the second stage.

IV. DESIGN OF PROPOSED MULTIPLE OUTPUT SMPS

In order to simulate the performance of proposed bridgeless buck –boost converter based SMPS it is important to find to out the values of the entire component. To obtain the proposed design all the diodes and switches are considered as ideal. The switching frequency selected here is very high as compared to the line frequency.

4.1 Design of Buck–Boost Converter

Input ac supply is directly given to this filter. The purpose of design of this filter is to reduce higher order harmonics also it reduces the distortion from ac supply. So in this L-C type maximum value of capacitor is calculated as[5],

$$Cin\ max = \frac{Im \tan\theta}{\omega Vm}$$

Where Vm and Im are the peak ac voltage and current. By substituting all the values we get 409nF.for θ value is considered 1° for maximum value of capacitor.

In order to maintain the low ripple at input ac side inductor value is given as below,

$$Lin = \frac{1}{4 * \pi^2 * fc^2 * Cin}$$

Where fc is a cutoff frequency. Thus value for inductor is obtained as3.07mH.A 2.5-mH filter inductor is selected for the hardware development.

Design Of Bridgeless Buck–Boost PFC Converter

The inductors present in the configuration of buck –boost converter are essentially designed in such way that they will ensure discontinuous conduction mode of operation. Inductor value is calculated bases on change in inductor current in one switching cycle is zero, ripple current is given as,

$$Lp = \frac{DTVavg}{\Delta iLpon}$$

Where D is duty ratio,T-total period, Vavg-average value of input voltage. In DCM in inductor ripple is maximum which is equal to the twice the input current,

$$\Delta iLpon = 2 * Iin$$

Thus by substituting all values inductor is calculated as 607µH but to ensure DCM inductor value is considered as 60 µH for switching time 50µS.

Design of Half-Bridge VSI

The input capacitors of the half-bridge VSI act as a low-pass filter to eliminate the harmonics, which is reflected due to the single-phase ac mains.

1) Design of Input Capacitor: The input capacitor is designed to eliminate the harmonics introduced due to the singlephase ac mains. Thus, it is governed by the amount of the 100-Hz (lowest harmonic) current flowing in the capacitor. For maintaining PFC operation, the input current and voltage should be in phase. Therefore, the input power Pin [3] is

$$Pin=\sqrt{2}VinSin\omega t*\sqrt{2}IinSin\omega t=VinIin(1-Cos2\omega t)$$

Where the latter term corresponds to the 100-Hz ripple which is reflected on the input capacitors of the half-bridge VSI

V. COMPARISON WITH OTHER EXISTING BRIDGELESS TOPOLOGIES

Table III shows the comparison of the proposed SMPS with other bridgeless buck–boost-converter-based SMPS systems.

Table IIIcomparison of the proposed SMPS with other bridgeless buck–boost-converter

Configuration	Components				Half cycle conduction
	Diode	Capacitor	Inductor	Switch	
Bridgeless SEPIC* [6]	2	4	3	2	10
Bridgeless Cuk Converter [7]	2	3	3	2	7
Bridgeless Cuk Converter [8]	3	2	3	2	8
Bridgeless Buck-boost Converter [9]	4	3	1	3	8
Proposed*	4	2	2	2	6

*Two output capacitors are considered.

An excellent performance of the proposed bridgelessconverter-based multiple-output SMPS is observed during steady-state condition, varying input voltages and loads in bothsimulation and test results. Hence, it can be unequivocally stated that the proposed converter can be adopted for SMPS applications for PCs.[6]

VI. CONCLUSION

The bridgeless based converter multiple output SMPS gives the better efficiency and good power quality performance at steady state as well as varying input voltage conditions. All the power quality measurements are well within the limits set by IEC-3-2.This SMPS gives the better voltage regulation due to use of buck-boost converter .Operation of buck boost converter in discontinuous mode gives better power factor and reduction in the total harmonic distortion.As the number of component used has reduced so switching losses as well as conduction losses are minimized. The multiple output SMPS maintained constant voltage irrespective of changes in the load voltage or deviations in supply voltages. This SMPS shows more reasonable result than conventionally SMPS so it is recommended solution to computer power applications.

REFERENCE

[1] N. Mohan, T. M. Undeland, and W. P. Robbins, Power Electronics: Converters, Applications and Design. Hoboken, NJ, USA: Wiley,2003.

[2] Limits for Harmonic Current Emissions, International Electro Technical Commission Standard, Std. 61000-3-2, 2004.

[3] IEEE Recommended Practices and Requirements for Harmonics Controlling Electric Power System, IEEE Std. 519, 1992.

[4] D. O. Koval and C. Carter, "Power quality characteristics of computerloads," IEEE Trans. Ind. Appl., vol. 33, no. 3, pp. 613– 621,May/Jun. 1997.

[5] V. Vlatkovic, D. Borojevic, and F. C. Lee, "Input filter design for power factor correction circuits," IEEE Trans. Power Electron., vol. 11, no. 1, pp. 199–205, Jan. 1996.

[6] E. H. Ismail, "Bridgeless SEPIC rectifier with unity power factor and reduced conduction losses," IEEE Trans. Ind. Electron., vol. 56, no. 4, pp. 1147–1157, Apr. 2009.

[7] A. A. Fardoun, E. H. Ismail, A. J. Sabzali, and M. A. Al-Saffar, "New efficient bridgeless Cuk rectifiers for PFC applications," IEEE Trans. Power Electron., vol. 27, no. 7, pp. 3292–3301, Jul. 2012.

[8] M. Mahdavi and H. Farzaneh-Fard, "Bridgeless Cuk power factor correctionrectifierwithreducedconductionlosses,"IETPowerElectron.,vol.5, no. 9, pp. 1733–1740, Sep. 2012.

[9] W. Wei, L. Hongpeng, J. Shigong, and X. Dianguo, "A novel bridgeless buck–boost PFC converter," in Proc. IEEE PESC, Jun. 15–19, 2008, pp. 1304–1308.