

LOW DROPOUT REGULATOR WITH LOW QUIESCENT CURRENT AND DROPOUT VOLTAGE

Praveenkumar¹, A R Priyarenjini², Manjunath R³

^{1,2,3}ECE, MSRIT, Bangalore, (India,)

ABSTRACT

Recent days on-chip power management become a very important thing for examples mobile phone battery is not lasting for a day, its draining out very fast so development of power management unit is important and in that category LDO comes in picture. LDO is a device which consumes less voltage and current and regulates power supply with less noise and this is used in many electronic gadgets like mobile phones, ipod, ipad, tv and computer and in many analog circuits and communication units. Input voltage is 1 V and got quiescent current (I_q) of about 5 μ A, with dropout voltage of 3 μ V and its designed in 90nm technology.

Keywords: LDO –Low DropOut component.

I. INTRODUCTION

The LDO Regulator is used in many applications like automotive, portable, medical, industrial applications. The automotive and medical circuits requires low dropout regulator to give power to the digital and analog circuits. Demand for battery operated devices are increasing tremendously for example cellular phones, video recorders and digital cameras. In a phone, switching regulators are used to increase the voltage but LDO's are used to suppress the noise with switchers. LDO's have advantage from working with low input and output voltages because power consumption is reduced by power calculation $\text{Power} = \text{load current (I)} * \text{Input voltage (V}_{in})$. Fig 1 shows components of LDO namely, a pass device, a voltage reference circuit, a feedback network, an Error amplifier

II. PROPOSED WORK IMPROVED

PERFORMANCE PARAMETERS

A LDO regulator consists of mainly four blocks namely an error amplifier (EA), a power MOS transistor (MP), a bandgap reference circuit (BGR) and a feedback network as shown in Fig. 1. At the output side LDO regulator consists of load capacitor (CL) and resistor (R_{SER}) in order to compensate for the stability of the circuit. Some of the improved performance parameters are discussed in the following sections.

2.1 Very less dropout voltage and Quiescent current (I_q)

The dropout voltage of LDO is given by the difference between the input and the output voltage. Quiescent current is the difference between the input and the output current. For a good LDO both these should be very less. The dropout voltage is directly proportional to the maximum load current of the

circuit. Hence by choosing the maximum load current as less as possible we can achieve very less dropout voltage. If dropout voltage decreases means the Quiescent current also decreases to very low value in the circuit.

2.2 High Stability through LDO compensation

Here the power MOS MP contributes a non-dominant pole at a low frequency. To make up for stability i.e. to cancel this non-dominant poles, a equivalent series resistance of RSER (CL) is required to produce a low frequency zero.

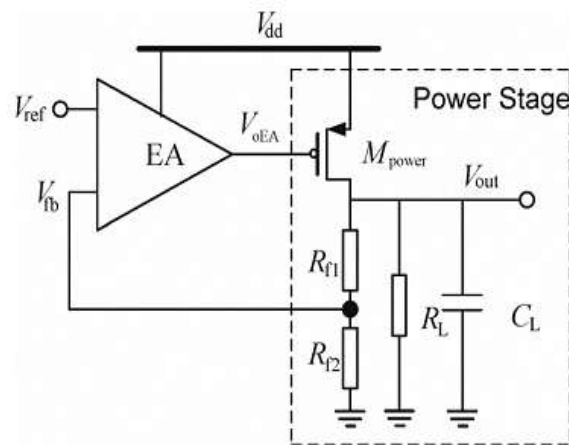


Fig 1: Schematic of LDO

III. LDO CIRCUIT DESIGNING

LDO regulator consists of four blocks and designing of all four blocks are explained in the following sections.

3.1 Error Amplifier

Two stage error amplifier is shown in fig 2. In two stage amplifier first stage is M1, M2, M3, M4 acts as differential amplifier, these transistors selected based in high gain bandwidth product and second stage M6, M7 acts as common source follower. By knowing the bias current transistor M5 and M7 are designed, and to achieve good phase margin compensation capacitor Cc is used. Gain of the error amplifier must be high in order to get good result, gain is calculated using following equations

$$A_{v1} = \frac{g_{m1}}{g_{ds1} + g_{ds4}}$$

$$A_{v2} = \frac{g_{m6}}{g_{ds6} + g_{ds7}}$$

$$\text{Total gain} = A_{v1} + A_{v2}$$

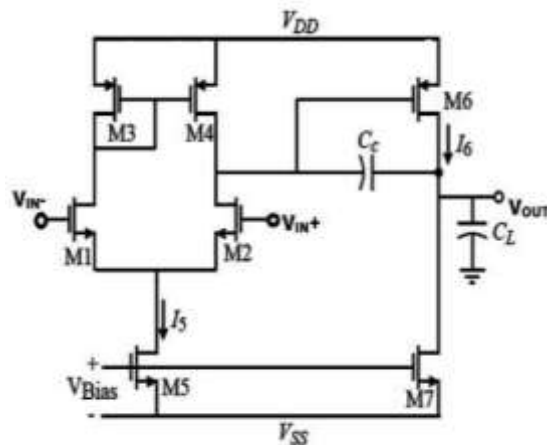


Fig.2. Two stage Error amplifier (EA)

3.2 Pass Transistor

Pass transistor used is PMOS because it has less threshold voltage, it has high aspect ratio and maximum aspect ratio is designed considering maximum load current and dropout voltage. The relation between load current and dropout voltage is

$$V_{\text{dropout}} = \sqrt{\frac{2I_{\text{max}}}{\mu_p C_{\text{ox}} \left(\frac{W}{L}\right)_p}}$$

3.3 Bandgap Reference(BGR)

Bandgap reference provides the constant reference voltage and this voltage is independent of temperature changes and supply voltage. Supply independent biasing is achieved through following equation

$$I_{\text{out}} = \frac{2}{\mu_n C_{\text{ox}} \left(\frac{W}{L}\right)_N} \cdot \frac{1}{R_s^2} \left(1 - \frac{1}{\sqrt{K}}\right)^2$$

Temperature independent biasing achieved through 1)Proportional to absolute temperature (PTAT) and 2)complementary to absolute temperature (CTAT), PTAT voltage one that varies positively with respect to temperature and CTAT voltage one that varies negatively with respect to temperature. fig3 shows the conventional BGR, BJTs Q1,Q2 acts as PTAT and Q3 Acts as a CTAT reference voltage generated is 0.5 V to 1.2V

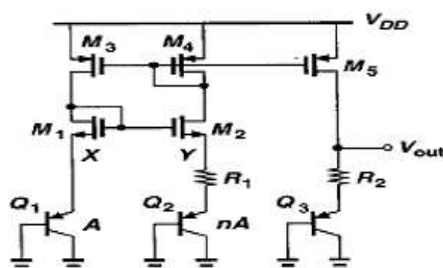


Fig 3 :Bandgap Reference Circuit

3.4 FeedBack Network Path

The feedback network path consists of two resistors R1 and R2. These resistors are designed by taking reference voltage from bandgap reference circuit and the regulated output voltage required and calculated by using following equation

$$V_{out} = \frac{(R_1 + R_2)}{R_2} * (V_{ref})$$

IV. IMPLEMENTATION AND RESULTS

Two Stage Differential Amplifier Is Designed In Cadence Virtuoso Schematic Editor Shown In Below Fig4. And Results In Fig5

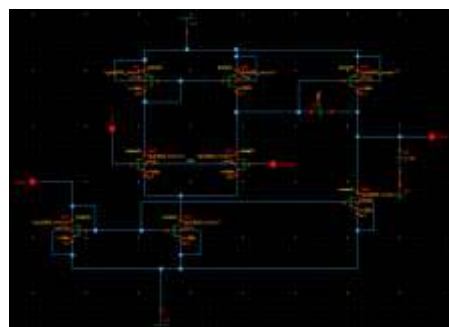


Fig 4: Two stage Error Amplifier(EA)

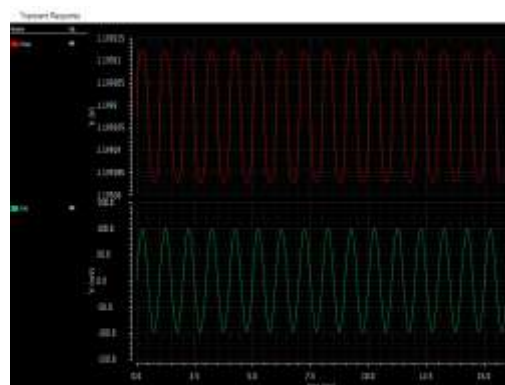


Fig5: Non-Inverting Output

Gain of the Error Amplifier obtained is 51.1dB and results shown below fig6

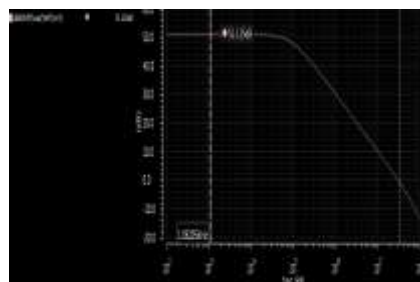


Fig6: Gain of Error Amplifier

Bandgap reference is designed and schematic showed in fig7

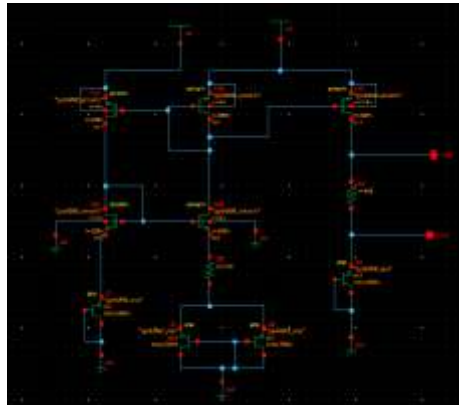


Fig 7: Schematic of Bandgap reference(BGR)

Computational result of Bandgap reference are shown in fig8

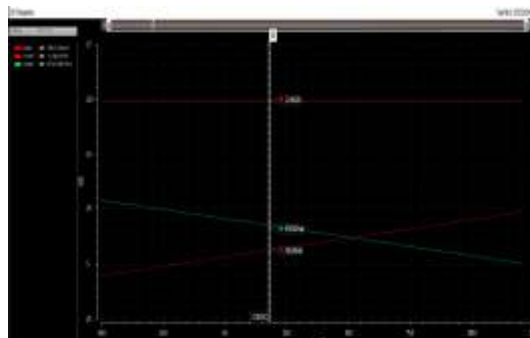


Fig 8: Output waveform of BGR

LDO regulator created in cadence virtuoso schematic editor and schematic of complete LDO shown in fig9



Fig 9: LDO Schematic

Waveform of voltage drop and input voltage



Fig10: LDO output voltage waveform



V. CONCLUSION

The proposed LDO which works with very low dropout voltage of about 3mV and less quiescent current of 5 μ A which are the characteristics of good LDO. The LDO output is constant to temperature and supply variation as reference voltage for regulator is taken from BGR circuit. The designed LDO can be used to provide stable voltages in the range from 0.5V to 0.997V and it is used as source voltage for many circuits and for circuits working in sub 1V operation.

REFERENCES

- [1] Jiangpeng Wang, Jinguang Jiang et al, on “ultra low noise and high psr ldo design” ASIC (ASICON), 2013 IEEE 10th International Conference, 1-4, Oct. 2013.
- [2] Robert J. Milliken, J S Martinez et al, “full on chip cmos ldo voltage regulator” IEEE transaction on circuits and systems, vol 54, sep 2007.
- [3] Jianping Guo, Ka Nang Leung et al “a 25ma cmos ldo with -85db psrr at 2.5mhz” IEEE Asian Solid-State Circuits Conference, 381-384, 2013.
- [4] Yali Shao, Yi Wang , Zhihua Ning , Lenian He, et al, “analysis and design of high power supply rejection ldo” IEEE 8th International Conference on ASIC, 324-327, 2009.
- [5] Yongqiang Xiao, Wengao Lu, Meng Chen, Yacong Zhang, Zhongjian Chen, et al, “a low noise, fast set-up low-dropout regulator in 65nm technology” Electron Devices and Solid State Circuit (EDSSC), 2012 IEEE International, 1-3, (2012)
- [6] Karim El Khadiri and Hassan Qjidaa Et al, “a low noise, high psr low-dropout regulator for low-cost portable electronics” ACS International Conference on Computer Systems and Applications, 1-5, 2013.
- [7] Zushu Yan¹, Liangguo Shen², Yuanfu Zhao¹, et al, “a low-voltage cmos low-dropout regulator with novel capacitor-multiplier frequency compensation” IEEE International Symposium on Circuits and Systems , 2685-2688, (2008).