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TSMC-CMOS TECHNOLOGY BASED HIGH SPEED LOW POWER PULSE TRIGGERED FLIP FLOP

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ABSTRACT

Practically, clocking system like flip-flop (FF) consumes large portion of total chip power as high as 50%. In this brief, a novel low-power pulse-triggered flip-flop (P-FF) design is presented. Here an explicit type pulse-triggered structure and a modified true single phase clock latch based on a signal feed-through scheme is used. Pulse-triggered FF (P-FF) is a single-latch structure which is more popular than the conventional transmission gate (TG) and master-slave based FFs in high-speed applications by solving the long discharging path problem in conventional explicit type pulse-triggered FF (P-FF). All low power flip flops (FF) proposed are supplied with a supply voltage (V_{DD}) ranging from 0.6v to 1.2v. Based on post-layout simulation results using TSMC CMOS 90-nm technology, the proposed design outperforms the conventional P-FF design. This paper concludes with the future challenges that must be met to design low power, high performance systems.

Keywords: Flip-Flop (FF), Pulse Triggered, TSMC CMOS

I. INTRODUCTION

Flip-flops (FFs) are the basic storage elements used extensively in all kinds of digital designs. In particular, digital designs nowadays often adopt intensive pipelining techniques and employ many FF-rich modules such as register file, shift register, and first in first out. It is also estimated that the power consumption of the clock system, which consists of clock distribution networks and storage elements, is as high as 50% of the total system power.

Pulse-triggered FF (P-FF), because of its single-latch structure, is more popular than the conventional transmission gate (TG) and master–slave based FFs in high-speed applications. Besides the speed advantage, its circuit simplicity lowers the power consumption of the clock tree system. A P-FF consists of a pulse generator for strobe signals and a latch for data storage. If the triggering pulses are sufficiently narrow, the latch acts like an edge-triggered FF. Since only one latch, as opposed to two in the conventional master–slave configuration, is needed, a P-FF is simpler in circuit complexity.

This leads to a higher toggle rate for high-speed operations [3]–[8]. P-FFs also allow time borrowing across clock cycle boundaries and feature a zero or even negative setup time. To obtain balanced performance among power, delay, and area, design space exploration is also a widely used technique [10]–[13]. In this brief, we present a novel low-power P-FF design based on a signal feed-through scheme. Observing the delay discrepancy in latching data “1” and “0,” the design manages to shorten the longer delay by feeding the input signal directly to an internal node of the latch design to speed up the data transition. This mechanism is implemented by

introducing a simple pass transistor for extra signal driving. When combined with the pulse generation circuitry, it forms a new P-FF design with enhanced speed and power-delay-product (PDP) performances.

II. CONVENTIONAL TYPE P-FF DESIGNS

2.1. Conventional Explicit Type P-FF Design

PF-FFs, in terms of pulse generation, can be classified as an implicit or an explicit type. In an implicit type P-FF, the pulse generator is part of the latch design and no explicit pulse signals are generated. In an explicit type P-FF, the pulse generator and the latch are separate [7]. Without generating pulse signals explicitly, implicit type P-FFs is in general more power-economical. However, they suffer from a longer discharging path, which leads to inferior timing characteristics. Explicit pulse generation, on the contrary, incurs more power consumption but the logic separation from the latch design gives the FF design a unique speed advantage.

Its power consumption and the circuit complexity can be effectively reduced if one pulse generator is shares a group of FFs (e.g., an n-bit register). In this brief, we will thus focus on the explicit type P-FF designs only. To provide a comparison, some existing P-FF designs are reviewed first. Fig. 1 shows a classic explicit P-FF design, named data-close to- output (ep-DCO) [7]. It contains a NAND-logic-based pulse generator and a semi dynamic true-single-phase-clock (TSPC) structured latch design. In this P-FF design, inverters I3 and I4 are used to latch data, and inverters I1 and I2 are used to hold the internal node X.

The pulse width is determined by the delay of three inverters. This design suffers from a serious drawback, i.e., the internal node X is discharged on every rising edge of the clock in spite of the presence of a static input "1." This gives rise to large switching power dissipation. To overcome this problem, many remedial measures such as conditional capture, conditional recharge, conditional discharge, and conditional pulse enhancement scheme have been proposed.

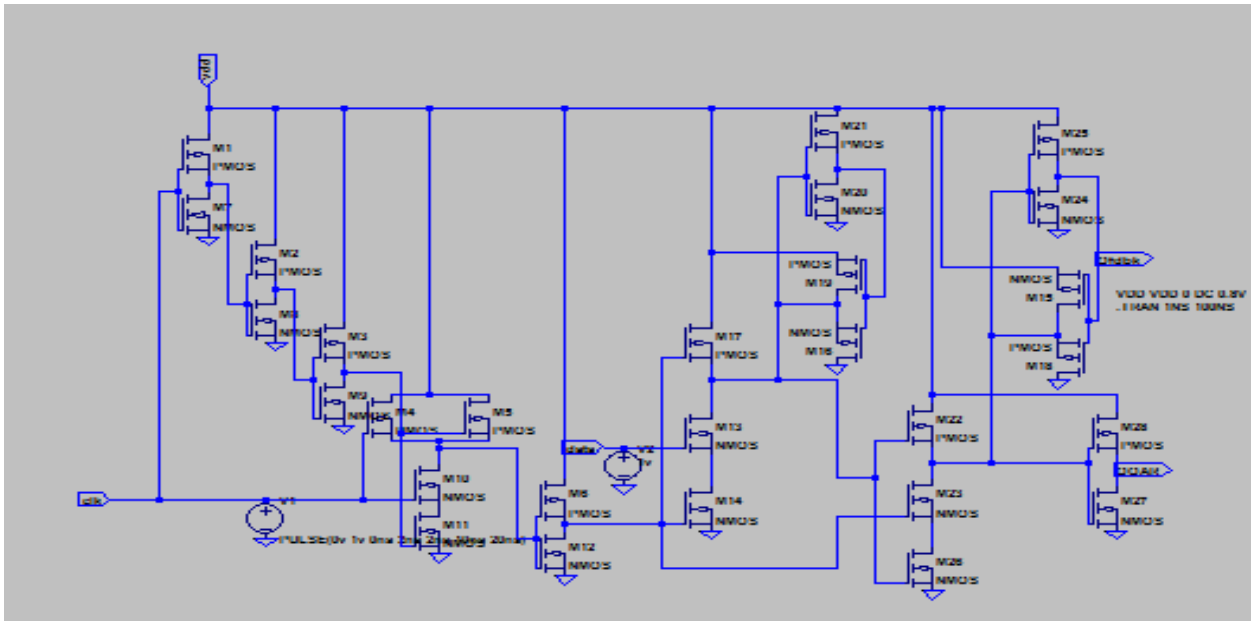

Fig1. Conventional Explicit Type P-FF Designs

2.2 CDFF

An extra nMOS transistor MN3 controlled by the output signal Q feedback is employed so that no discharge occurs if the input data remains "1." In addition, the keeper logic for the internal node X is simplified and consists of an inverter plus a pull-up PMOS transistor only.

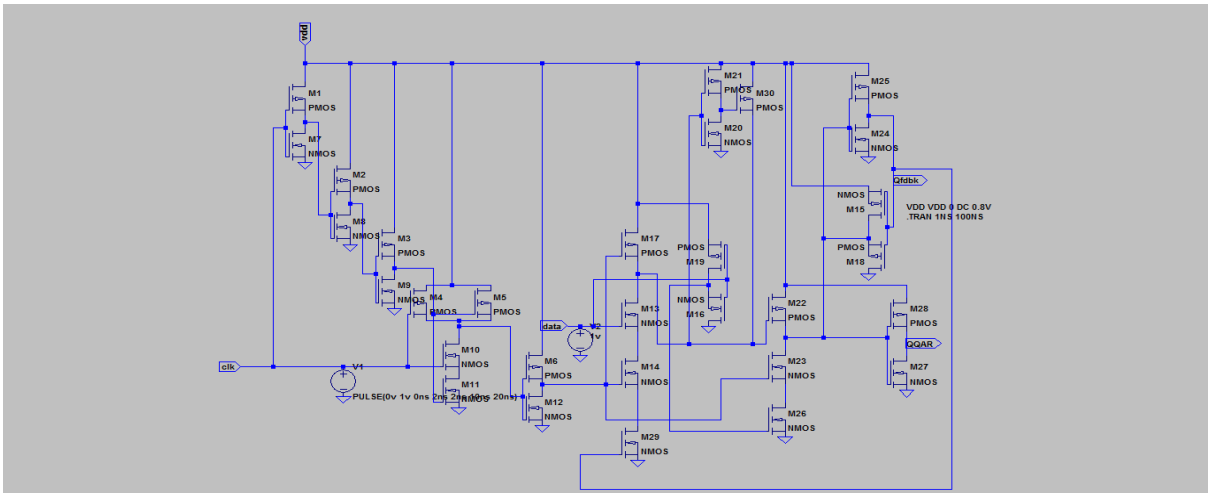

Fig2. Shows a conditional discharged (CD) technique

2.3 STATIC-CDFF

Figure 3 shows a similar P-FF design (SCDFF) using a static conditional discharge technique. It differs from the CDFF design in using a static latch structure. Node X is thus exempted from periodical recharges. It exhibits a longer data-to-Q (D-to-Q) delay than the CDFF design. Both designs face a worst case delay caused by a discharging path consisting of three stacked transistors, i.e., MN1–MN3. To overcome this delay for better speed performance, a powerful pull-down circuitry is needed, which causes extra layout area and power consumption. The modified hybrid latch flip-flop (MHLFF) [19] shown in Fig. 1(d) also uses a static latch. The keeper logic at node X is removed. A weak pull-up transistor MP1 controlled by the output signal Q maintains the level of node X when Q equals 0. Despite its circuit simplicity, the MHLFF design encounters two drawbacks. First, since node X is not pre discharged, a prolonged 0 to 1 delay is expected. The delay deteriorates further, because a level-degraded clock pulse (deviated by one VT) is applied to the discharging transistor MN3. Second, node X becomes floating in certain cases and its value may drift causing extra dc power.

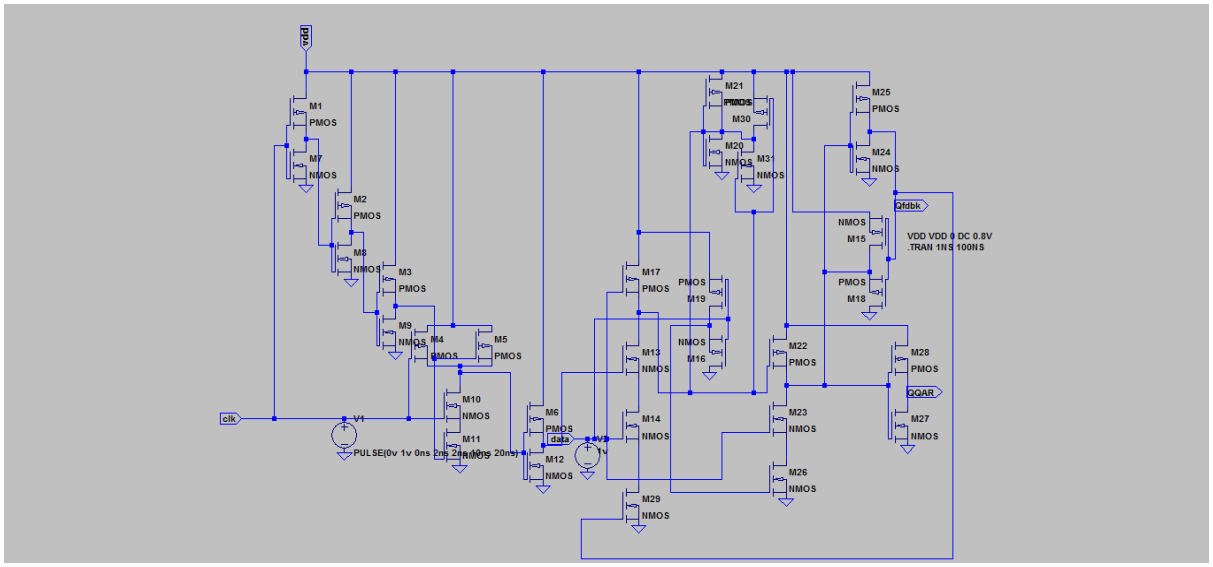

Fig3. Static conditional discharge technique

2.4 MHLFF

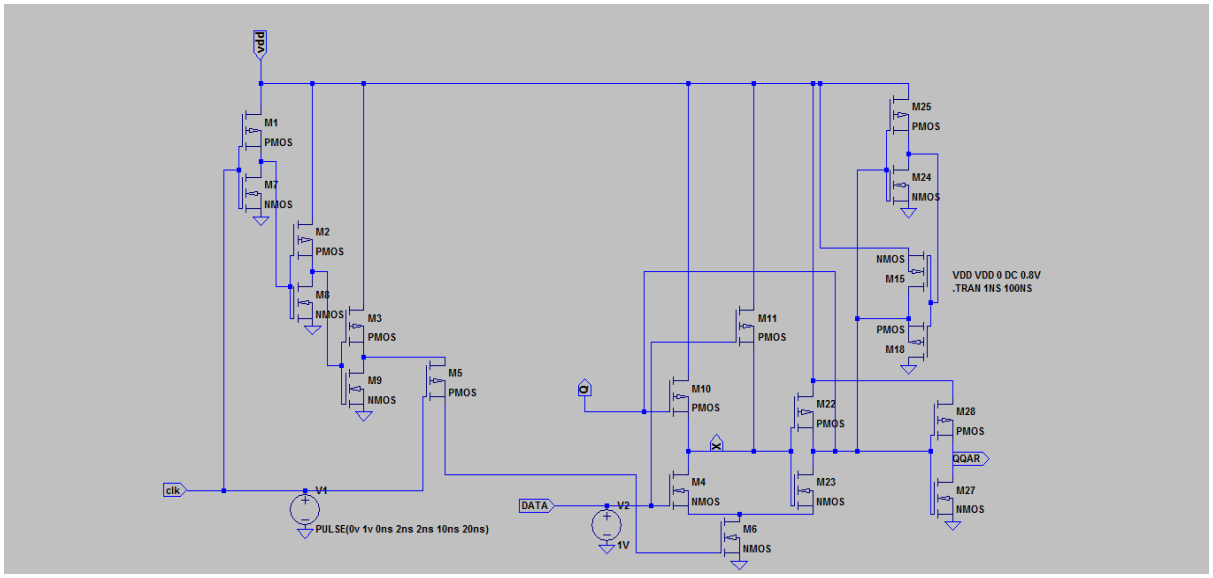

Fig4. Modified Hybrid latch flip flop

The modified hybrid latch flip-flop (MHLFF) [19] shown in Fig. 4 also uses a static latch. The keeper logic at node X is removed. A weak pull-up transistor MP1 controlled by the output signal Q maintains the level of node X when Q equals 0. Despite its circuit simplicity, the MHLFF design encounters two drawbacks. First, since node X is not pre discharged, a prolonged 0 to 1 delay is expected. The delay deteriorates further, because a Level-degraded clock pulse (deviated by one VT) is applied to the discharging transistor MN3. Second, node X becomes floating in certain cases and its value may drift causing extra dc power [18].

III.PROPOSED P-FF DESIGN

Recalling the four circuits reviewed in Section II, they all encounter the same worst case timing occurring at 0 to 1 data transitions. Referring to Fig. 5, the proposed design adopts a signal feed-through technique to improve this delay. Similar to the SCDFF design, the proposed design also employs a static latch structure and a

conditional discharge scheme to avoid superfluous switching at an internal node. However, there are three major differences that lead to a unique TSPC latch structure and make the proposed design distinct from the previous one. First, a weak pull-up pMOS transistor MP1with gate connected to the ground is used in the first stage of the TSPC latch. This gives rise to a pseudo-nMOS logic style design ,and the charge keeper circuit for the internal node X can be saved .In addition to the circuit simplicity, this approach also reduces the load capacitance of node X [20], [21].Second, a pass transistor MNx controlled by the pulse clock is included so that input data can drive node Q of the latch directly (the signal feed-through scheme).Along with the pull-up transistor MP2 at the second stage inverter of the TSPC latch, this extra passage facilitates auxiliary signal driving from the input source to node Q. The node level can thus be quickly pulled up to shorten the data transition delay. Third, the pull-down network of the second stage inverter is completely removed. Instead, the newly employed pass transistor MNx provides a discharging path. The role played by MNx is thus twofold, i.e., providing extra driving to node Q during 0 to 1 data transitions, and discharging node Q during "1" to "0" data transitions. Compared with the latch structure used in SCDFF design, the circuit savings of the proposed design include a charge keeper, a pull-down network and a control inverter .The only extra component introduced is an nMOS pass transistor to support signal feed through.

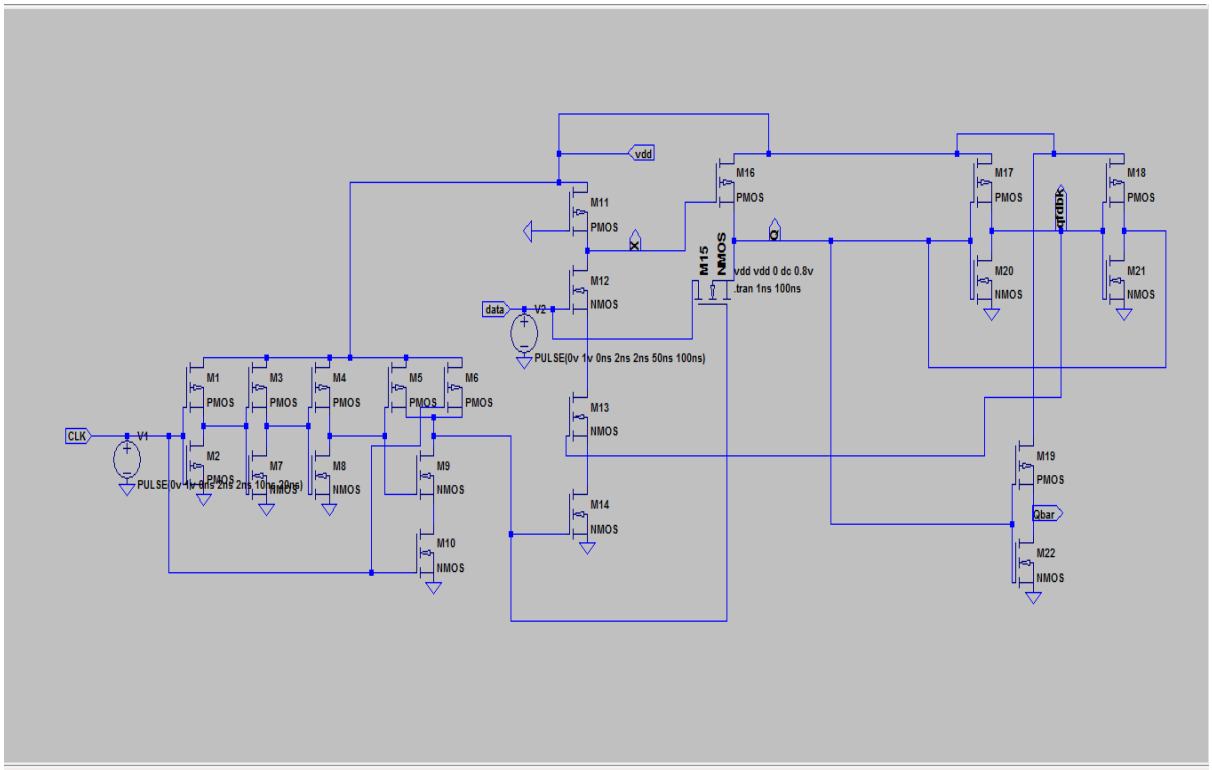

Fig5. Schematic of Proposed Pulse- Triggered Flip-Flop

IV. COMPARISON OF VARIOUS FF DESIGNS

Performance of FF Designs design does not use the least number of transistors; it has the smallest layout area. This is mainly attributed to the signal feed-through scheme, which largely reduces the transistor sizes on the discharging path. In terms of power behavior, the proposed design is the most efficient in five out of the six test patterns. The savings vary in different combinations of test pattern and FF design. For example, if a 25% data

switching test pattern is used, the proposed design is more power economical than all except the ACFF design. Its power saving against ep-DCO, CDFF, SCDFF and MHLFF are 22.7%, 6.9%, 8.1% and 8.3% respectively [16]. The ep-DCO design consumes the largest power because of the superfluous internal node discharging problem. ACFF design [2] power efficiency is even more significant in the cases of zero or low input data switching activity.

Similarly, another non-P-FF design, the TGFF, performs lightly better than the proposed one in the case of static input patterns (0% switching activity). However, when a test pattern with 100%switching activity is applied, the proposed deign is 9% and 12%more power efficient than the ACFF design and the TGFF design, respectively. This can be explained by the power overhead of the pulse generator regardless of the data patterns in all P-FF designs. The significance of this overhead, however, decreases as the data switching activity increases. The leakage powers of all FF designs under different combinations of clock and input signals. A possible concern on the proposed design arises from the pseudo-nMOS logic in the first stage. Although an always-on MP1 prevents node X from full voltage swing, it does not result in any dc power consumption problem. Since the proposed signal feed-through scheme requires occasional signal driving from the input node directly to the output node, we also calculate the power drawn by the pass transistor MNx (the extra power consumption caused by the signal feed through scheme).Post-layout simulation results show that this part accounts for only8.47% of the total power consumption when the input data switching activity is 100%. The percentage reduces to 1.62% when the input data switching activity is lowered to 12.5%.Finally the lay out decreased with 24 number of transistors.

TABLE. Feature Comparison of Various FF Designs

FF designs	ep - DCO	CDFF	SCDFF	MHLFF	PROPOSED
Numbers of transistors	28	30	31	19	24
Lay out area (μm²)	76.99	89.70	88.99	77.97	69.01
Setup time (ps)	-84.56	-88.91	-44.67	1.49	-84.76
Hold time (ps)	110	123.4	122.9	93.5	119.9
Minimum D to Q Delay(ps)	117.9	129.6	140.0	172.9	108.9
Average Power (100% Activity)μW	34.01	34.07	35.04	31.07	30.99
Supply voltage (VDD)v	0.8	0.8	0.8	0.8	0.6

V. SIMULATION RESULTS

The performance of the proposed P-FF design is evaluated against existing designs through post-layout simulations. A conventional CMOS NAND-logic-based pulse generator design with a three-stage inverter chain [as show in Fig. 1] is used for all P-FF designs except the MHLFF design, which employs its own pulse generation circuitry as specified in Fig.4. The target technology is the TSMC 90-nm CMOS process. Since pulse width design is crucial to the correctness of data capture as well as the power consumption [10]–[13], the transistors of the pulse generator logic are sized for a design spec of 120 ps in pulse width in the TT case. The

sizing also ensures that the pulse generators can function properly in all process corners. With regard to the latch structures, each P-FF design is individually optimized subject to the product of power and D-to-Q delay. To mimic the signal rise and fall time delays, input signals are generated through buffers. Since the proposed design requires direct output driving from the input source, for fair comparisons the power consumption of the data input buffer (an inverter) is included. The output of the FF is loaded with a20-pf capacitor. An extra loading capacitance of 3 pf is also placed at the output of the clock buffer [18]. The operating condition used in simulations is 50 MHz/0.6v to 50MHz/1.2v

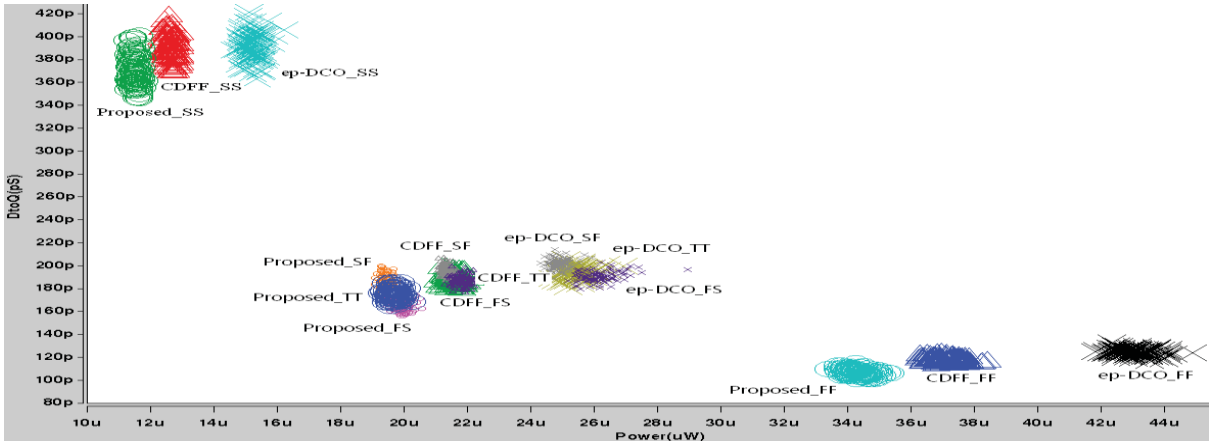

Fig6. Monte Carlo simulation results

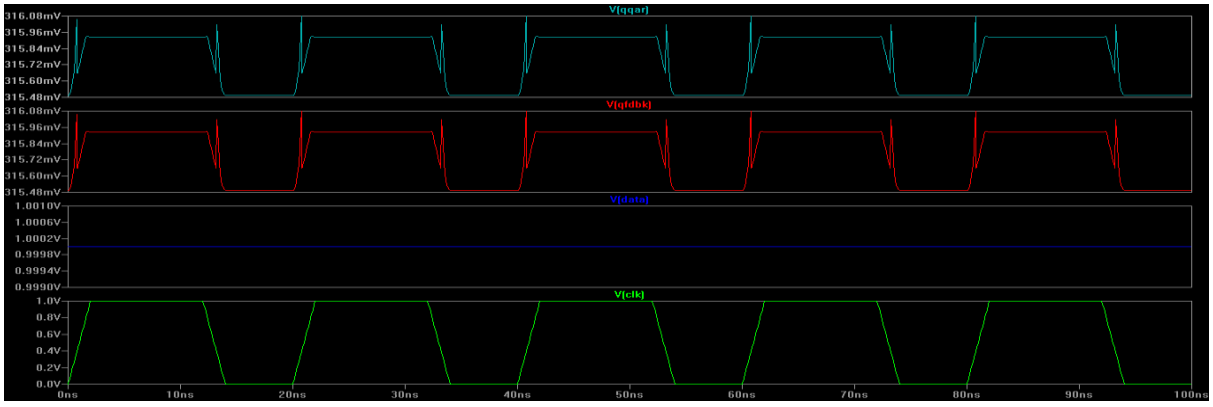

Fig7.EP-FF simulation results

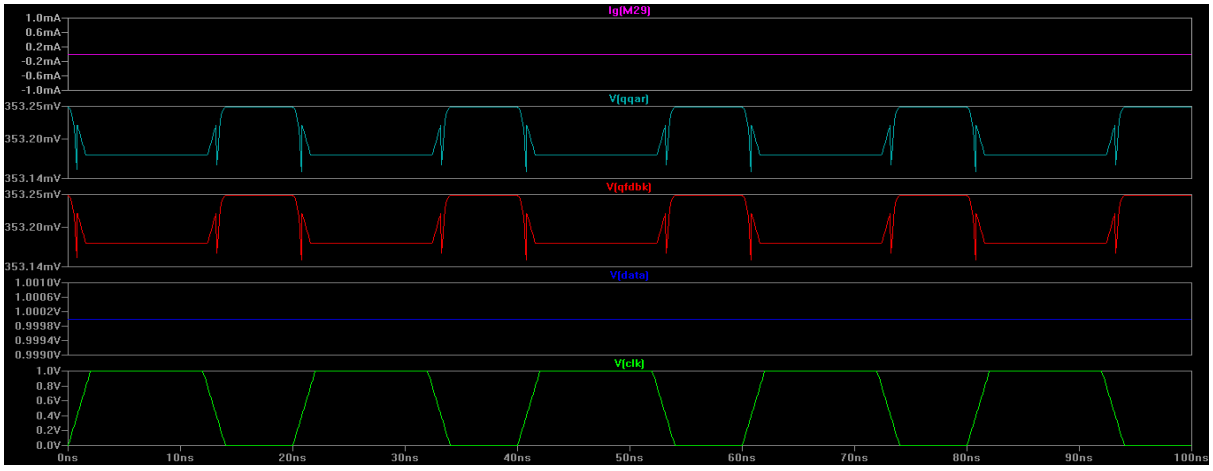

Fig8. CDFF simulations results

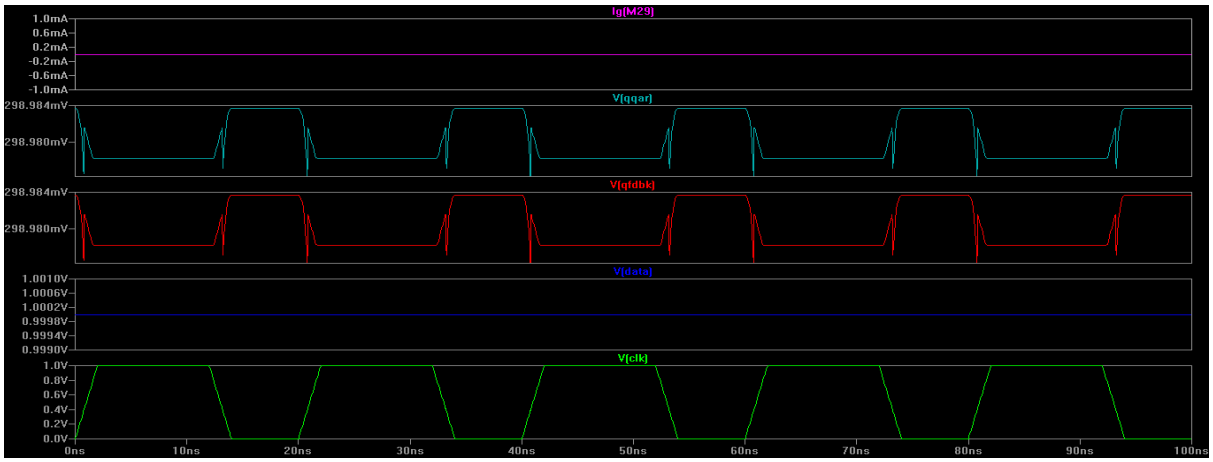

Fig9. Static-CDFF simulation results

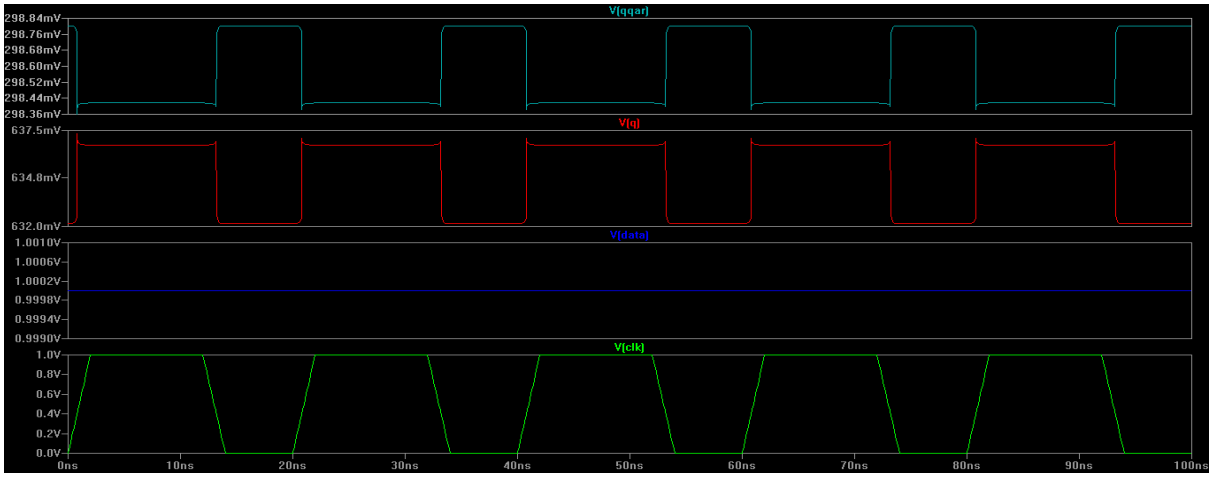

Fig10. MHLFF simulation results

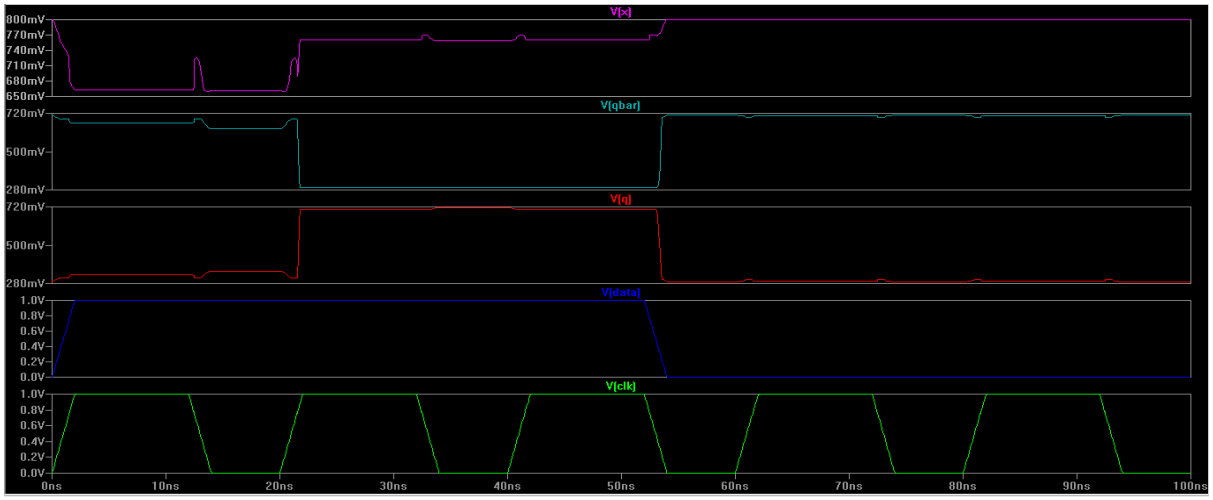

Fig11. Proposed PFF Design Simulation Results

VI. CONCLUSION

In this brief, we presented a novel P-FF design by employing a modified TSPC latch structure incorporating a mixed design style consisting of pass transistor and pseudo-nMOS logic. The key idea was to provide a signal

feed through from input source to the internal node of the latch, which would facilitate extra driving to shorten the transition time and enhance both power and speed performance. Supply voltage is mainly dependent on low power dissipation in future p-FF design by employing a modified latch structure. The design was intelligently achieved by employing a simple pass transistor. Extensive simulations were conducted, and the results did support the claims of the proposed design in various performance aspects.

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