International Journal of Advance Research in Science and Engineering
Vol. No.4, Issue No. 12, December 2015
www.ijarse.com
IJARSE
ISSN 2319 - 8354

NOVEL ENCODING APPRAOCHES FOR THE ELIMINATIG DATA TRANSISTIONS ON NOC APPLICATIONS

Chilakala Tejavathi[1], D.Suneel[2]

[1]Pursuing M.tech, [2]Asst.Professor (ECE), Nalanda Institute of Engineering and Technology(NIET), Siddharth Nagar, Kantepudi village, Sattenepalli Mandal Guntur Dist.,A.P. (India)

ABSTRACT

The network on chip is the communication strategy used to communicate between the various elemnts on SOC. The power and area is the main concern for scaling the devices, when the technology is scaling down the power consumed by the links and power consumed by the various elements in communication media such as routers and network interfaces will use comparable amount of power. To redcue total system power we need reduce the power consumed by either links or either routers. In this paper we adopted thet technique to reduce the energy of links by using set of encoding schemes at the router such that data transmission over the links will be in encoded passion. So that this encoding techniques will reduce the transistion in the links, which in turns reduce the energy.

Keywords: Data encoding schemes, Network on chip(NOC), Odd inversion, Even inversion.

I. INTRODUCTION

The SOC will have more number of devices will be connected on single die which makes faster and power efficient gates but they need wires to interconnect them on SOC. These wires usually consume half of the total power consumed by the circuit. The wires will have RCcomponents which inturns introduces delay in the propagation path still the size of chip will be the same. The SOC which has the capablitity of accompanying more and more number of cores on single die but to work with sytem present on the die needs communication between the cores. This paper concern about the power consumed by the links having equal amount as power consumed by the routers and interfaces.when the technology is growing down that consumed by links may also be consumed more. To reduce that power we are introducing set of data encoding schemes which will reduce the switching activites namely self switching and coupling switching activity. These encoding schemes will reduce the coupling switching activity by making data transfer in linear passion. In this encoding schemes data will be operated either flit level or end to end basis data transfer over the links in network.

II. BACKGROUND AND RELATED WORK

The power consumed by the network is completely due to the interconnection circuitry. Most of the designs are concentrated to reduce the power consumed by different parts of the interconnections. Those are NIs,routers and

links. The previous designs are concentrated to reduce power of links that suggests shielding to the link, introduce the large space between the lines and inserting repeaters even they need more area but the othet techniques are data encoding techinques there are several encoding techniques which reduces the power without introducing the area. Those encoding techniques may reduce any one of switching technique either coupling switching or self switching. The self switching activity is that power consumed by the same bus due to data transfer in it. The bus inversion and inc-xor coding styles are employed to reduce power for randomly distributed data patterns. We also employ other coding like gray code, one zone encoding and T0-XOR gate for the correlated data pattern. Since each data will have unique style of data transitions hence employing different techniques. This techniques will not suitable for the data transfer at the submicrometer techonology nodes where each node is having certain capacitance, that capacitance will constitue major portion of the power dissipation at the nodes. This iscalled coupling switching.

The other type of switching is coupling is switching is power consumed by one bus due to data transfer in other adjacent bus capacitance. To reduce this switching we may add few extra control lines which will reduce the switching but the decoding logic is quite complex. Even there are special ways to avoid coupling transistions are presented in several previous works but they were failed. We discuss few of the works as one encoding technique consider the data transfer in flit level, the data flits will betraversed through the link, the encoder will count number of 0 to1 transitions through the link. If the transistions are higher than the link width data inversion will takes place on the traversed flits there by reducing the self switching activity. The state of art in the silicon techonolgy the coupling capacitance will have larger effect link power consumption.

To reduce that power we use one encoding technique where we have to reduce the coupling transitions by employing one encoder at each node since that data transfer is considered as hop hy hop approach,in that we have to employ encoder and decoder at each node. So according to this strategy encoder is used to calculate the number of type-I tarsnsitions with the weighting factor of one and weighting factor two for type-II transistions at the node. If this number is greater than the half of the link width the inversion will be performed to redcue such type of transitions accordingly. The full inversion will be performed on specific data pattern whose inversion will save the links power consumption, where as some data pattern this type of inversion will increase the link power consumption hence it is failed. In other method we sent bits as the in the form bunches of fourbit and it is encoded as five bits as a group, the five bit group is arranged in passion to avoid interaction between them by providing shielding between them to avoid 101 ans 010 transistion in the adjacent pair of bits such that occurrence of type –II transistion at the same time is avoided. This will redcue the coupling switching effcectively but increase the data transfer time which incrases delay. This in turn leads to more link energy consumption. To make effective link power reduction we adopted end-end basic data transfer of warm hole switching by using these techniques we will eleiminate the type-II transistions completely such that it is implemented.

The propsed method will comprises of three schemes , the first method or scheme used to count type –I transistions and scheme second is used to identify type –Iand type-II transistions accordingly we may invert either half or full depend upon the situation which leads to highest power savings. The third scheme will makes one of three inversions either half or full depend on the count of the encoder present at that node.

III. IDEA OF PROPOSED SYSTEM

the idea behind the proposal is data has to be encoded prior to the sending into the network aimed to reduce the self switching and coupling switching. These two activities are prime reason for power dissipation in the link when data is traversed through it. Here we are following the end to end scheme. This will have advantage that it can use pipelining process for the warm hole switching process. The encoding process done at the NI to reduce the amount of switching. In the proposed method we employ encoder and decoder at NI. The whole data flit will be encoded except the header flit such that amount switching reduce to reduce the link power consumption

IV. PROPOSED METHOD OF ENCODING SCHEMES

In this proposed method we describe three encoding shemes aimed to reduce the link power disspation by redcuing the coupling and self switching activities. We discussing about the power consumption so we have to check for the dynamic power consumption, the dynamic power consumption P

$$P = [T_{0\rightarrow1}\ (Cs + Cl\ ) + TcCc]\ v^2_{dd}\ f_{ck}$$

The $T_{0\rightarrow1}$ number of 0 to1 transision in the two consecutive data transfers, Tc is the number which represents number of correlated data pattern between physically adjacent lines. The substrate capacitance is denoted by the Cs and the load will have also some capacitance is denoted by Cl. Every device must have some power supply inorder to perate it that is denoted by Vdd. The speed of the operation is denoted by the clock frequency. Basically we may classify four types of transitions type-I,Type-II,Type-III,and Type-IV. The type-I transistion in which any one lines has to be switched other has to be consatnat. When one of the line will make change from high to low and other line will make change as low to high i.e when both lines changing as vice –versa it is called type-ii switching. When both lines changing simulataneously in same manner is belongs to type –iii, whereas for type –iv there must be no change in the links in which data is transferring. The coupling capacitance have main reason is its node capacitance we call it as switched capacitance which will be very different from one type to another type. So we say the total coupling transition is due to all types of switching so we have to sum up all transistion with some weighing factor to get exact figure that is denoted by

$$Tc = K1T1 + K2T2 + K3T3 + K4T4$$

$T1$, $T2$ $T3$ $T4$ denotes the which type transitions they corresponding to type-I,type-II,Type-III and Type-IV.where as K1,K2,K3,K4 represnts respective weighing factors of them. We usually consoder from the previous works as $K1 = 1$, $K2 = 2$, and $K3 = K4 = 0$. We assume the probabilities of the random data patterns as 1/2 and 1/8 which leads the type -1 transistion will have greater impact on the link power saving.

$$P = [T_{0\rightarrow1}\ (Cs + Cl\ ) + (T_1+2T_2)Cc]\ v^2_{dd}\ f$$

We can caluate the probabilities of happening different type of transitions, the bit flits which already passed through the link is denoted by the flit(t-1), the current flit which is ready to pass through the link is denoted as flit(t), we consider two bits in present flit and two bits on the previous flit which cummulatievly four bits and sixteen combinations will be possible, they all are catagiroised as Type-I,Type-II,Type-III, Type-IV. They will have 8,2,2 and 4 four in number for random set of data pattern.

For the random set of adata pattern probabilities of occcurnce of the above types are ½,1/8,1/8 and ¼.

International Journal of Advance Research in Science and Engineering
Vol. No.4, Issue No. 12, December 2015
www.ijarse.com
IJARSE
ISSN 2319 - 8354

A. Scheme One

Under this sheme we are going to invert type-I and type-II transistion either may odd invert or not,depend upon the count at the Encoder output. The type-I and type-II transitions are conveterd to type-III and type-IV such that transistions will be avoided. This is accomplished by comparing current passing data with the previously encoded data depend upon them inversion or no inversion will be performed.

If we say the flit is odd inverted then its corresponding power consumption i.e dynamic power is given as

$$P \propto T\,0\rightarrow1+ K1T1+ K2T2+ K3T3+ K4T\,4Cc$$

T 0→1, $T1$,$T2$, $T3$, T 4, The first term represents self transitions and coupling transtiotion of fourtypes respectively.

Time	Normal			Odd Inverted		
	Type I			Types II, III, and IV		
$t-1$	00, 11	00, 11, 01, 10	01, 10	00, 11	00, 11, 01, 10	01, 10
t	10, 01	01, 10, 00, 11	11, 00	11, 00	00, 11, 01, 10	10, 01
	T1*	T1**	T1***	Type III	Type IV	Type II
$t-1$	Type II			Type I		
t	01, 10			01, 10		
	10, 01			11, 00		
$t-1$	Type III			Type I		
t	00, 11			00, 11		
	11, 00			10, 01		
$t-1$	Type IV			Type I		
t	00, 11, 01, 10			00, 11, 01, 10		
	00, 11, 01, 10			01, 10, 00, 11		

Table-I: Coupling Transitions and Detailed Types and their Effectd when Odd Inversion is Performed

The above table represents the four types of transition and how they will be changed when if odd inversion is perfomed. The (t-1) represents previous flit, fist bit represents the ith link data, second bit represents i+1 link data in the group.From the table we say that if type-II,III,IV odd inversions will convert the data to type-I transitions whereas odd inversion of type-I transition is giving various other type of transitions namely divided as below T1*,T1**,T1***.

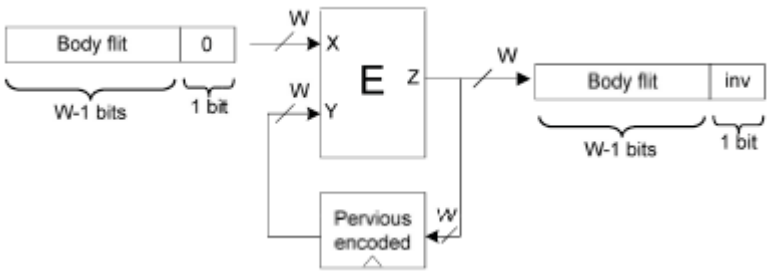


Fig Generic block diagram for the Encoder

International Journal of Advance Research in Science and Engineering
Vol. No.4, Issue No. 12, December 2015
www.ijarse.com
IJARSE
ISSN 2319 - 8354

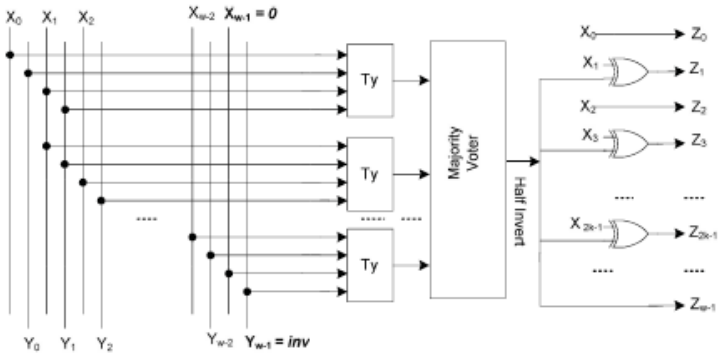


Fig Scheme-I Encoder

$P \propto (T0 \rightarrow 0(\text{odd}) + T\,0 \rightarrow 1(\text{even}))Cs + [K1\,(T2+T3+T4) + K2T1^{***} + K3T\,1^{*} + K4T1^{**}]Cc$ Then we say that if P is grater than P' definetly we have to make odd inversionto redcue the link power dissipation of the network. Hence we deduce the expression for the odd invert condition ¼ $T\,0 \rightarrow 1 + T1 + 2T2 > 1/4(T\,0 \rightarrow 0(\text{odd}) + T\,0 \rightarrow 1(\text{even})) + T2 + T3 + T4 + 2T\,1^{***}$ we can also write above equatiuon is as follows ¼ $T0 \rightarrow 1(\text{odd}) + T1 + 2T2 > 1/4\ T\,0 \rightarrow 0(\text{odd}) + T2 + T3 + T4 + 2T\,1^{***}$ We want to find the exact condition for the odd inversion has to performed as we write approximate the exact condition as follows $T1 + 2T2 > T2 + T3 + T4 + 2T1^{***}$ by making approximation we may become inefficient due to the approximation errors in the analysis, but they greatly reduces the hardware architecture of the encoder which is the benefit, for that we have to define few terms as . $Tx=T3+T4+T1^{***}$ *and* $Ty = T2 + T1 - T1^{***}$we can write as $Ty > Tx$. We say that W which represents the width of the link. The total number of transition possible in the adjacent lines are (w-1) $Ty + Tx = w - 1$.The condition for the odd inversion is

$$Ty > \frac{(w-1)}{2}$$

The proposed Encoding architecture is based on the odd inverting condition,let w be the width of the link,the encoding which is embedded inside the network interface. The NI will accumulutae the body flits together with w-1 bit, the w bit is used to represent whether the flit is inverted or not. The common block diagram is same for all three scheme but the encoding logic is different. The inverting decision will be taken at the Encoder, that is accomplished by comparing previously encoded flits with current flit is compared at the network interface, the inversion will be performed. The Encoder will have Ty block which will have four inputs one from the current link and other from the previous link. The inputs (x1,x2..) are the current inputs for the Tyblock. The Y1,Y2…are the inputs from the previous link. The inv bit is present in the previous encoded flit. This bit in the previus encoded flit will be used for denoting whether this flit is inverted or not. The Ty block will identify inversion is possible, if possible how it will be performed. The Ty block will identify the transitions, if the data belongs to Ty transition then it will produce output will be one other wise output will be logic zero. Then next stage will be majority block which will identify the condition for odd inversion, if it gets satisfied the last stage will perform odd inversion which leads to the link power reduction.

B. Scheme Two

In this scheme we concentrate on type-II transition by performing odd and full inversions that data will be converted to type-IV transitions. The inversion decission will be taken up by the encoder comparing the current

flit with the previous encoded flit.The various dyanmic powers associated with each inversion odd , full or no inversion is given as follows *P, P', P''* the odd inversion is efficient in the case when $P' < P''$ and $P' < P$

$$P \propto T1 + 2T4 **$$

If we neglecting the self switching activity then the powers $P' < P''$

$$T2 + T3 + T4 + 2T1** < T1 + 2T4 **$$

We may write the following equation as S2

$$(T2 - T\,4**) < 2Ty - w + 1$$

The odd inversion condition is we find as follows from the above eqautions2

$$(T2 - T\,4**) < 2Ty - w + 1\ Ty > (w - 1)/2$$

We also need to find the condition for the full inversion that is possible iff $P'' < P'$ and $P'' < P$

$$T2 > T\,4**2\ (T2 - T\,4**) > 2Ty - w + 1\ T2 > T4**$$

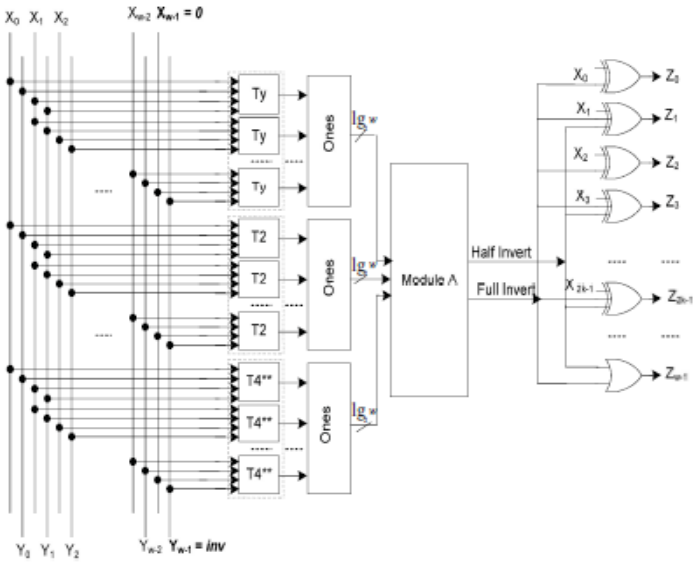


Fig Scheme-II Encoder

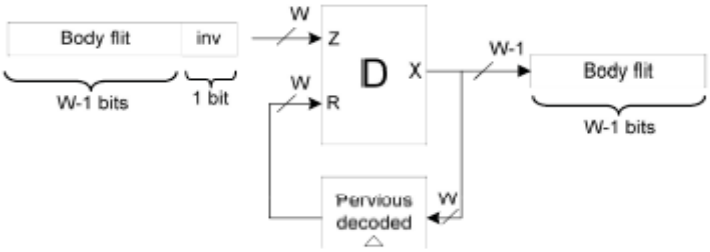


Fig Generic Block Diagram for the Encoder

International Journal of Advance Research in Science and Engineering
Vol. No.4, Issue No. 12, December 2015
www.ijarse.com
IJARSE
ISSN 2319 - 8354

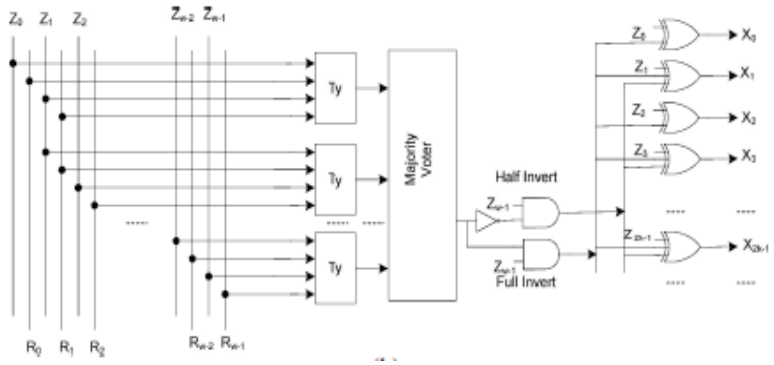


Fig Scheme-II Decoder

This encoding method will have odd and full inversion mechanisms in addition to the scheme on encoder depend upon the previous flit bit , the inversion will be performed. The wth bit of the previous flit denoted with inv, which indaictes the inversion is performed or not on the previous flit. The T2,T4 blocks are added additionally to the Tyblock, the T2,T4** blocks identifies the type2 and type4 transistionwhich gives condition for full inversion, where as Ty blocks give condition for odd inversion. The first stage compreises of above blocks with inputs of current previous data flits from the links then they will be identified them, if they detects particular type of transitions then that block will give output as one otherwise it will give as zero. The second stage will consist of set of one's blocks they will calculate number of ones present for each transition block. There are three ones block each for one transition. The top ones block will give condition for number of transitions that leads to odd inversion to reduce link power, middle one block give condtion for number of tarnsition possible for full inversion which leeads linl power reduction. The final ones block will give us number of transition for full inversion which leads link power increase. The third stage will consist of module A which is a combination of full adder and comparator. This will take decession on which inversion has to be performed. There are outputs for Module A will decide the inversion phenomenon based on condition listed above for full and odd inversions, if it is odd inversion then first bit will be one ,else for full inversion both of the outputs has to be one and for no inversion both will be zero. Then last stage will perform inversion according to the outputs given by ModuleA.

The simple decoder architecture is presented here it will have only Ty block and inputs will be same as previously decoded data with w-1 bits, wth bit represnted by inv bit, this indicates that either it is inverted or not. Ty block identifies that which type of transition are present in the encoded signal. The majority block will identifies the validity of the encoded signal with invbit. The incoming encoded sifnal is denoted as Zi(Ri) which are previous encoded signals. After getting output from the majority block that will be decoded with logic gates and effect of inv bit.

C .Scheme Three

In the proposed encoding scheme we have added even inversion inaddition to the odd and full inversion which makes effcient link power reduction. While making odd inversion some of type-I transitions are becoming type-II transitions, that makes it inefffcient. The even inversion of those types transitions becoming type-III and type-IV which is an effcient way for them as shown in table-II. That reduces the link power energy. This accomplished with the comparison of previous encoded flit to the current flit.When the message flit is

transmitted over the link the dynamic power consumed by the link for no,odd , even and full inversion respectievly as P, P', P'', P'''For odd inversion the condition will be as

$$T1 + 2T2 > T2 + T3 + T4 + 2T\,1*$$

We may define even invert block Te as $Te = T2 + T1 - T1*$

We get the condition for $P''' < P$

$$Te > (w - 1)/2$$

For odd and fullinversion we will get the condition as $P'''<P'$

$$T2 + T3 + T4 + 2T1* < T2 + T3 + T4 + 2T\,1***$$

We can write the condition $Te > Ty$. Also we will get the condition

$$T2 + T3 + T4 + 2T1* < T1 + 2T\,4**$$

Now we have to define Tr and Te terms as $Tr = T3 + T4 + T1*$

$$Te = T2 + T1 - T\,1*$$

Let the link width of w bits and number of bits in data is w-1

$$Te + Tr = w - 1.$$

We may rearrange the equation2

$$(T2 - T\,4**) < 2Te - w + 1.$$

The even inversion is useful for power reduction when $P'''<P$, $P'''< P'$ and $P'''< P''$

$$Te>(w - 1)/2,\ Te>Ty\ ,$$

$$2\,(T2 - T\,4**) < 2Te - w+1$$

The full inversion is useful for power reduction when $P''<P'$, $P''< P''$ and $P''< P2$

$$(T2 - T\,4**) > 2Ty - w + 1,$$

$$(T2 > T4**)\ 2\,(T2 - T\,4**) > 2Te - w + 1.$$

The full inversion is useful for power reduction when $P'<P''$, $P'< P''$ and $P''< P'''$ 2

$$(T2 - T\,4**) < 2Ty - w + 1,$$

$$Ty > (w - 1)/2\ Te < Ty\ .$$

Time	Normal			Even Inverted		
	Type I			Types II, III, and IV		
$t-1$	01, 10	00, 11, 01, 10	00, 11	01, 10	00, 11, 01, 10	00, 11
t	00, 11	10, 01, 11, 00	01, 10	10, 01	00, 11, 01, 10	11, 00
	T1*	T1**	T1***	Type II	Type IV	Type III
$t-1$ t	Type II 01, 10 10, 01			Type I 01, 10 00, 11		
$t-1$ t	Type III 00, 11 11, 00			Type I 00, 11 01, 10		
$t-1$ t	Type IV 00, 11, 01, 10 00, 11, 01, 10			Type I 00, 11, 01, 10 10, 01, 11, 00		

Table-II: Coupling Transitions and Detailed Types nad their Effectd when Even Inversion is Performed

International Journal of Advance Research in Science and Engineering
Vol. No.4, Issue No. 12, December 2015
www.ijarse.com
IJARSE
ISSN 2319 - 8354

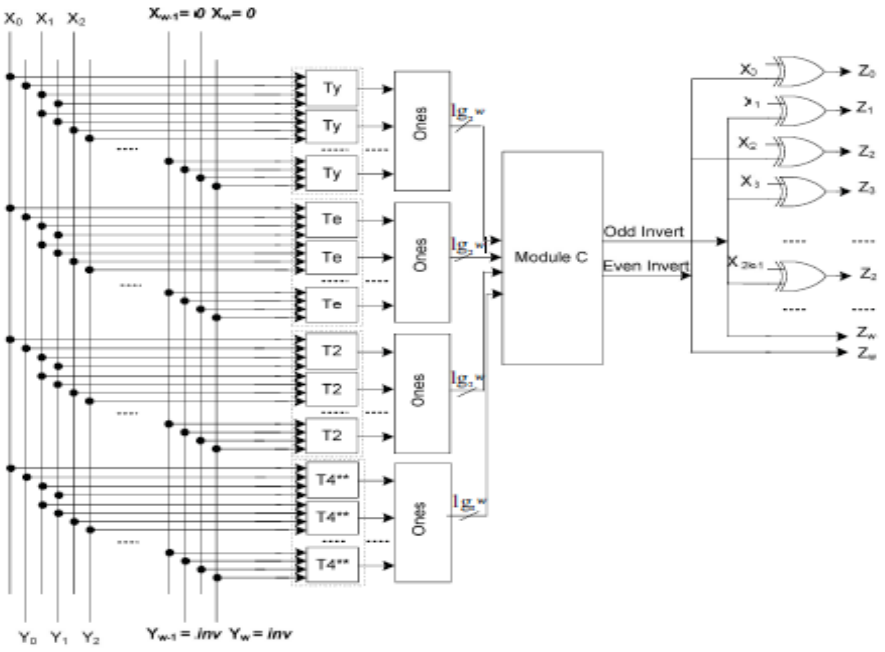


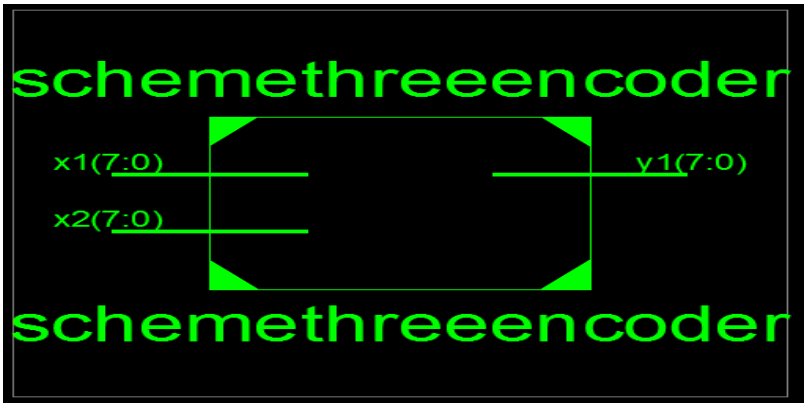
Fig Scheme-III Encoder

In the above scheme in addition to thescheme two encoder we are also added the even inversion which makes the design power efficient. The even inversion is efficient for such types of type-I transition which making them to type-3 and type-IV where there are less probable transitions. The first stage will have only previous encoded w-1 bits and wth bit as inveterd bit to represent whether the data is inverted or not. For Ty,T2,T4**,we added Te block which will identify the T2,T1**,T1***, and make them even inverted. Similarly to the scheme 2 the secondstage will have ones block. Each one block decided specific functionality odd,even full and no inversuions respectively. Those ones block outputs are fed back to the Module C which will decide the type of inversion has to takes place by its outputs as 00,01,10 and11 represents no,even, odd and full inversions respectievly.

V. SIMULATION RESULTS

Thepaper presents all transition types and its encoding techniques in three schemes with no, even, odd and full inversionspossible, all the schemes encoder are designed with Verilog HDL. Those RTL description checked and synthesized using XILINX ISE13.2 I. Those resepected designs are verified with FPGA and got the synthesis reports. From the reports we have found lesser number LUThas been utilized such that less power has been consumed for it.

5.1 Schematic Diagram



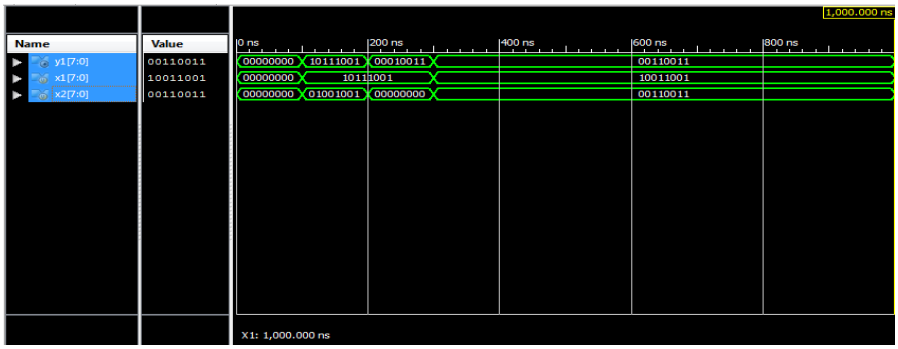
5.2 Synthesis Results

schemethreeencoder Project Status			
Project File:	dataencoding.xise	**Parser Errors:**	No Errors
Module Name:	schemethreeencoder	**Implementation State:**	Synthesized
Target Device:	xc7a30t-3csg324	**• Errors:**	No Errors
Product Version:	ISE 13.2	**• Warnings:**	10 Warnings (10 new)
Design Goal:	Balanced	**• Routing Results:**	
Design Strategy:	Xilinx Default (unlocked)	**• Timing Constraints:**	
Environment:	System Settings	**• Final Timing Score:**	

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice LUTs	43	21000	0%
Number of fully used LUT-FF pairs	0	43	0%
Number of bonded IOBs	24	210	11%

Detailed Reports					[-]
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	Thu 5. Nov 13:43:01 2015	0	10 Warnings (10 new)	7 Infos (7 new)
Translation Report					
Map Report					

5. Simulation Results



VI. CONCLUSION

This project present very efficient methods for avoiding all coupling transitions activites in the links. In this four types of transition are presented out of them type-I and type-II taking effective part of the power consumption.so in this project by making inversion tecgniues we have converted all type-I and type-II transitions into type-III and Type-IV which are less cause for link power consumption. To achieve this we proposed three schemes of

encoding techniques and their decoding techniques. From the synthesiesd results we say that these methods are effectively redcuing the transition in links when data traversed through them

RERERENCES

[1]. Data Encoding Techniques for Reducing Energy Consumption in Network-on-Chip Nima Jafarzadeh, Maurizio Palesi, Member, IEEE, Ahmad Khademzadeh, and Ali Afzali-Kusha, Senior Member, IEEE, IEEE Transactions On Very Large Scale Integration (Vlsi) Systems, Vol. 22, No. 3, March 2014

[2] L. Benini and G. De Micheli, "Networks on chips: A new SoC paradigm," Computer, vol. 35, no. 1, pp. 70–78, Jan. 2002

[3] International Technology Roadmap for Semiconductors. (2011) .

[4] A. Vittal and M. Marek-Sadowska, "Crosstalk reduction for VLSI," IEEE Trans. Comput.-Aided Design Integr. Circuits Syst., vol. 16, no. 3, pp. 290–298, Mar. 1997

[5] M. Ghoneima, Y. I. Ismail, M. M. Khellah, J. W. Tschanz, and V. De, "Formal derivation of optimal active shielding for low-power on-chip buses," IEEE Trans. Comput.-Aided Design Integr. Circuits Syst., vol. 25, no. 5, pp. 821–836, May 2006.

[6] L. Macchiarulo, E. Macii, and M. Poncino, "Wire placement for crosstalk energy minimization in address buses," in Proc. Design Autom. Test Eur. Conf. Exhibit., Mar. 2002, pp. 158–162.

[7] R. Ayoub and A. Orailoglu, "A unified transformational approach for reductions in fault vulnerability, power, and crosstalk noise and delay on processor buses," in Proc. Design Autom. Conf. Asia South Pacific, vol. 2. Jan. 2005, pp. 729–734.

[8] K. Banerjee and A. Mehrotra, "A power-optimal repeater insertion methodology for global interconnects in nanometer designs," IEEE Trans. Electron Devices, vol. 49, no. 11, pp. 2001–2007, Nov. 2002.

[9] M. R. Stan and W. P. Burleson, "Bus-invert coding for low-power I/O," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 3, no. 1, pp. 49–58, Mar. 1995.

[10] S. Ramprasad, N. R. Shanbhag, and I. N. Hajj, "A coding framework for low-power address and data busses," IEEE Trans. Very Large Sc

[11] L. Rung-Bin, "Inter-wire coupling reduction analysis of bus-invert coding," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 55, no. 7, pp. 1911–1920, Aug. 2008.

[12] Z. Khan, T. Arslan, and A. T. Erdogan, "Low power system on chip bus encoding scheme with crosstalk noise reduction capability," IEE Proc. Comput. Digit. Tech., vol. 153, no. 2, pp. 101–108, Mar. 2006.

[13] Z. Yan, J. Lach, K. Skadron, and M. R. Stan, "Odd/even bus invert with two-phase transfer for buses with coupling," in Proc. Int. Symp. Low Power Electron. Design, 2002, pp. 80–83.

[14] C. P. Fan and C. H. Fang, "Efficient RC low-power bus encoding methods for crosstalk reduction," Integr. VLSI J., vol. 44, no. 1, pp. 75–86, Jan. 2011.

[15] S. R. Vangal, J. Howard, G. Ruhl, S. Dighe, H. Wilson, J. Tschanz, W. James, D. Finan, A. P. Singh, T. Jacob, S. Jain, V. Erraguntla, C. Roberts, Y. V. Hoskote, N. Y. Borkar, and S. Y. Borkar, "An 80-tile Sub-100-W TeraFLOPS processor in 65-nm CMOS," IEEE J. Solid-State Circuits, vol. 43, no. 1, pp. 29–41, Jan. 2008.

AUTHOR DETAILS

	**CHILAKALA TEJAVATHI**, Pursuing M.tech in Nalanda Institute of Engineering and Technology, She completed her B.tech Electronics and Communication Engineering. Her research of intrest includes communication systems, Digital communications, Satelite communication etc
	**D.SUNEEL** , Working as assistant professors in Nalanda Institute of Engineering and Technology, He completed his Post Graduation,He has four years of teaching experience. Her research of intrest includes communication systems, Digital communications, Satelite communication etc