International Journal of Advance Research in Science and Engineering
Vol. No.4, Issue No. 12, December 2015
www.ijarse.com
IJARSE
ISSN 2319 - 8354

DESIGN OF 64-BIT ALU USING VEDIC MATHEMATICS FOR HIGH SPEED SIGNAL PROCESSING RELEVANCE'S

Srikanth Yellampalli[1], V. J Koteswara Rao[2]

[1]Pursuing M.tech (VLSI), [2]Asst. Professor (ECE), Nalanda Institute of Engineering and Technology (NIET), Siddharth Nagar, Kantepudi (V), Sattenpalli (M), Guntur Dist, A.P. (India)

ABSTRACT

Nowadays due to the growing demand for improving processor performance in handling the complex algorithms and multi functioning making the all processor cores are going to integrate on single chip. Even though the burden on the processor is not reducing. In order to reduce this we should provide the coprocessor for supporting operations done by main processor, these coprocessors will perform numeric operation like addition, multiplication, DSP application, etc. The speed of the processor will depend on the speed of the coprocessors. Vedic mathematics is the ancient type of mathematics which are having unique technique of 16 formulas to find solution of various application in the fast way. Here we are designing an ALU which was based on these maths using Verilog HDL and synthesised in Xilinx ISE 13.2, found that it's having enhanced performance.

***Keywords*: ALU, Vedic Mathematics, MAC, Nililam sutra**

I. INTRODUCTION

Vedic mathematics is the powerful mechanism provided by the ancient Indian scientists. This mathematics usually depicted in our Vedas by various sages. Swami Bharathi Krishna Acharya who was studied the Vedas and inspired from the mathematics and wrote a book concluding all the formulae's together from basic elementary maths to modern mathematics. Vedic maths is faster than modern maths, which provides calculation orally at faster rate, we can also done this on the paper. Vedic maths will work on the basis of 16 sutras and their upa sutras which allow students to compute in their own methods not only in specified way as like as in modern maths. It will allow us calculate solutions for all types of mathematical problems like basic maths to nonlinear partial differential equations etc.

Vedic the word comes from the word Vedas which means storage house of all knowledge. Its completely based on 16 sutras which covers wide range of fields like algebra, geometry etc. Those sutras are listed below

1. (Anurupye) Shunyamanyat – if one is zero other is ratio
2.Chalana-Kalanabyham – Differences and Similarities.
3. Ekadhikina Purvena – By one more than the previous one
4. Ekanyunena Purvena – By one less than the previous one

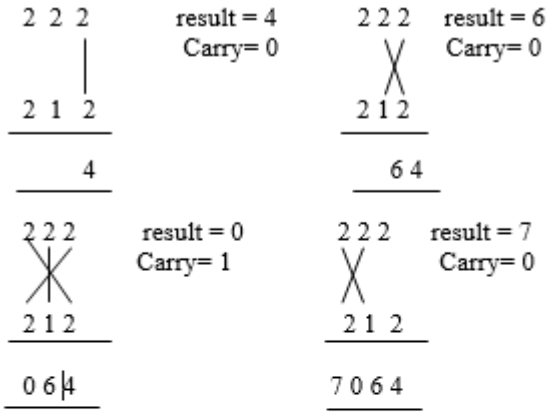
IJARSE
ISSN 2319 - 8354

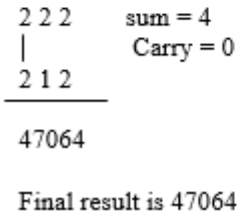
5. Gunakasamuchyah – The factors of the sum is equal to the sum of the factors.
6. Gunitasamuchyah – The product of the sum is equal to the sum of the product.
7. Nikhilam Navatashcaramam Dashatah – All from 9 and the last from 10.
8. Paraavartya Yojayet – Transpose and adjust.
9. Puranapuranabyham – By the completion or Non completion.
10. Sankalana-vyavakalanabhyam – By addition and by subtraction.
11. Shesanyankena Charmaine – The remainders by the last digit.
12. Shunyam Saamyasamuccaye – When the sum is the same that sum is zero.
13. Sopaantyadvayamantyam – The ultimate and twice the penultimate.
14. Urdhva-tiryakbyham – Vertically and crosswise.
15. Vyashtisamanstih – Part and Whole.
16. Yaavadunam – Whatever the extent of its deficiency

II. PROPOSED VEDIC TECHNIQUE

2.1 Urdhva-Tiryakbyham

The proposed algorithm uses two formulae's are Urdhva-tiryakbyham, Nikhilam Navatashcaramam Dashatah

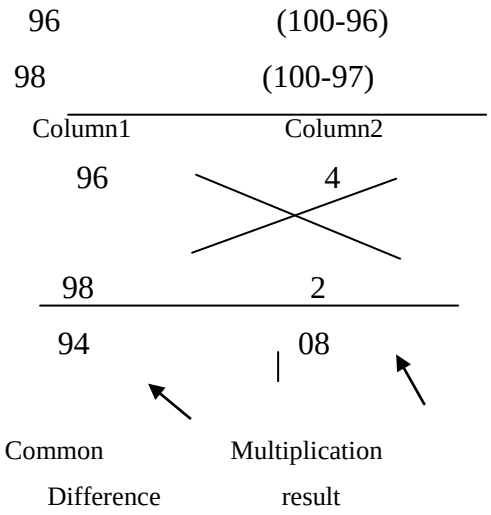




Final result is 47064

2.2 Nikilam Sutra

96 X 98



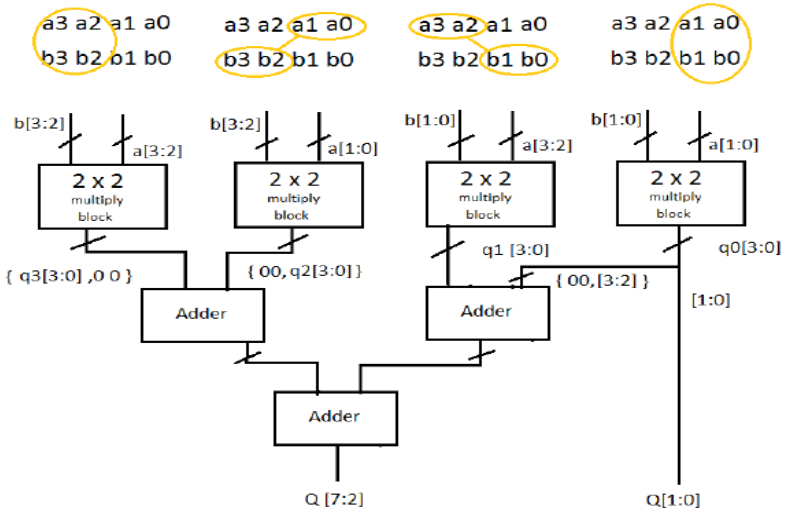
From the above we can explain the procedure as follows first we have to find compliments of the given numbers, compliments are nothing but result by subtracting the given number from its nearest base. We can say the bases as 10,100,100 etc. For the above nearest base is 100 so subtract the given numbers from 100, we get 2, 4, then we form 2 columns. Column 1 having given numbers and column 2 having their compliments. In the second step we form common difference by subtracting one number compliment with another number, make multiplication of their compliments. Results of common difference and multiplication together form overall result.

Nikilam sutra was described above by using example in decimal. it can be effectively applied for the instance of where operands are larger so that their compliments was smaller and we can easily find the result of them. For finding compliments we choose base as 10, 100, 1000.....etc. We can also apply this type of multiplication to the binary number system, we have designed an ALU which will work on the these principles.

2.3 Implementation of Higher Order Multipliers

In this project we are implementing 64bit multiplier in the 64 bit ALU. To design this 64 bit Multiplier, we have to know the architecture of the multiplier. From the architecture of the 2*2 multiplier we can develop 4*4 multiplier as with four 2*2 multipliers and with three adders. One adder contains 4 bits and second adder will contain six bit adder.

International Journal of Advance Research in Science and Engineering
Vol. No.4, Issue No. 12, December 2015
www.ijarse.com
IJARSE
ISSN 2319 - 8354



Similarly for 8*8 multiplier, we will use 4*4 multiplier as well and few adders with two different number of bits. To design n*n bit multiplier, we have to design n/2 bit multipliers first then we should have an n-bit adder, 2^n+2^{n-1} bit adders. First divide the string of data into two parts upper part and lower part of two operands. The first operand upper parts with two parts of the second operands are applied to n/2 multiplier. Similarly other parts will be applied to remaining two n/2 multipliers. Then products from the n/2 multiplier are shown added with simple addition structure to get the final product. The 64*64 bit multiplier needs 32*32 multiplier, 16*16 multiplier and 8*8 all architectures with simple mechanisms are presented below

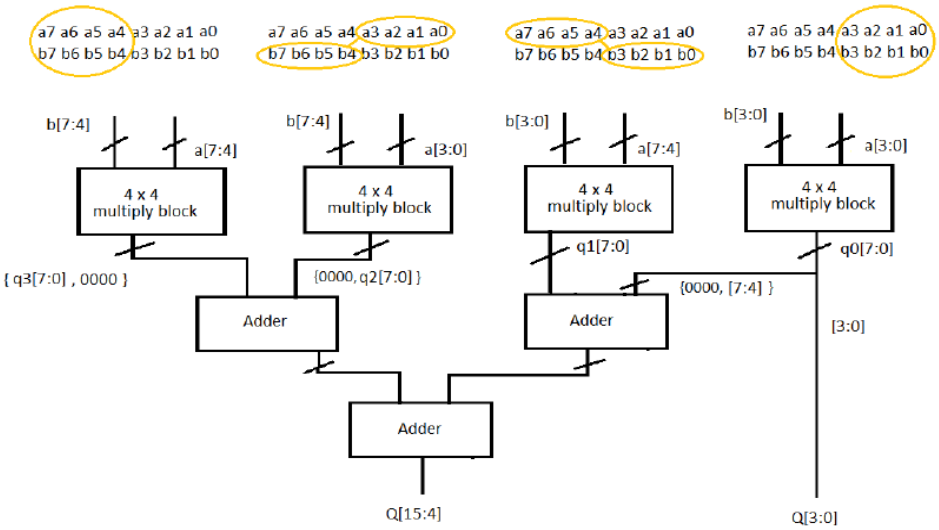


Fig 4.1 Proposed 8*8 Multiplier

International Journal of Advance Research in Science and Engineering
Vol. No.4, Issue No. 12, December 2015
www.ijarse.com
IJARSE
ISSN 2319 - 8354

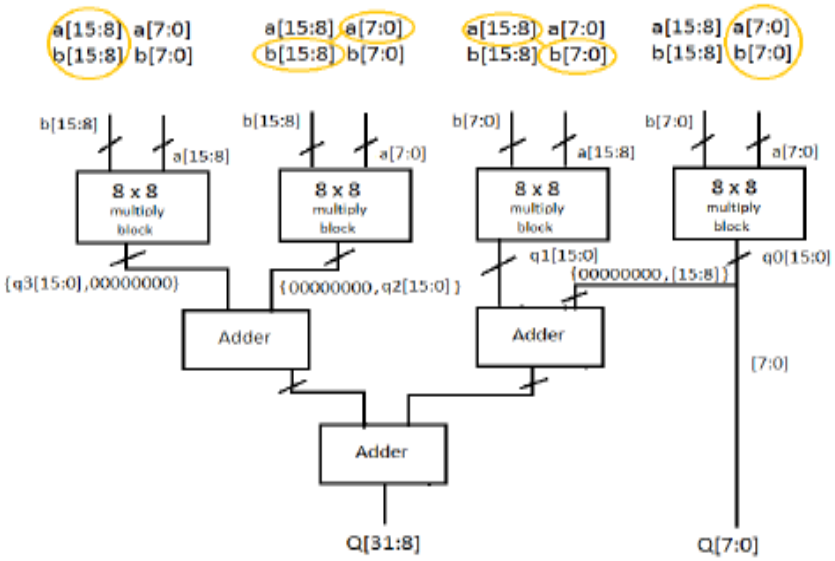


Fig 4.1 Proposed 16*16 Multiplier

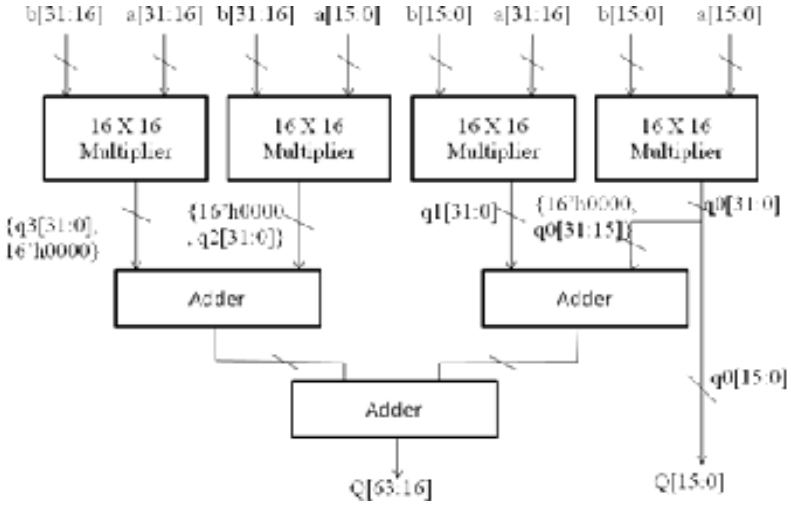


Fig 4.1 Proposed 32*32 Multiplier

III. MULTIPLY AND ACCUMULATE UNIT

Mac is the essential block in ALU, it will perform multiplication of two numbers and adds product to the result in the accumulator. Mac will generally present in the all computation units. The Mac will generally performs DSP operations like convolution, correlation, DFT, FFT etc. We will perform multiplier design using Vedic mathematics. So with this design we can achieve speed and area and reduce delay. It gives enhanced performance as well as consumes less power. We have integrated MAC and air thematic unit .Which will perform addition and subs traction and also Vedic multiplier were included in the design of ALU.

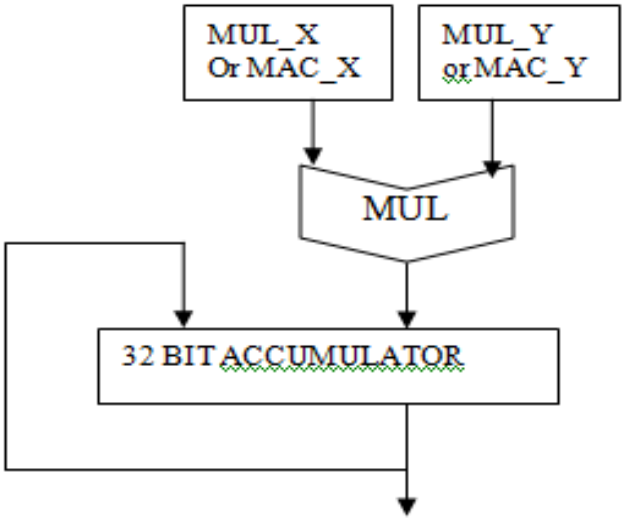


Fig 3.2 Block diagram of ALU

IV. IMPLEMENTATION OF ALU

The Proposed ALU consist of logical and unit and arithmetic units. The logical operators and arithmetic operators are connected to the Multiplexer. They possess same inputs and produces output based on the selection line of the user. We mainly concentrating in the design of the ALU with proposed Vedic multiplier which has very simple architecture with compared to the conventional Vedic multiplier. The proposed ALU has very sufficient amount of speed, area and power improvement.

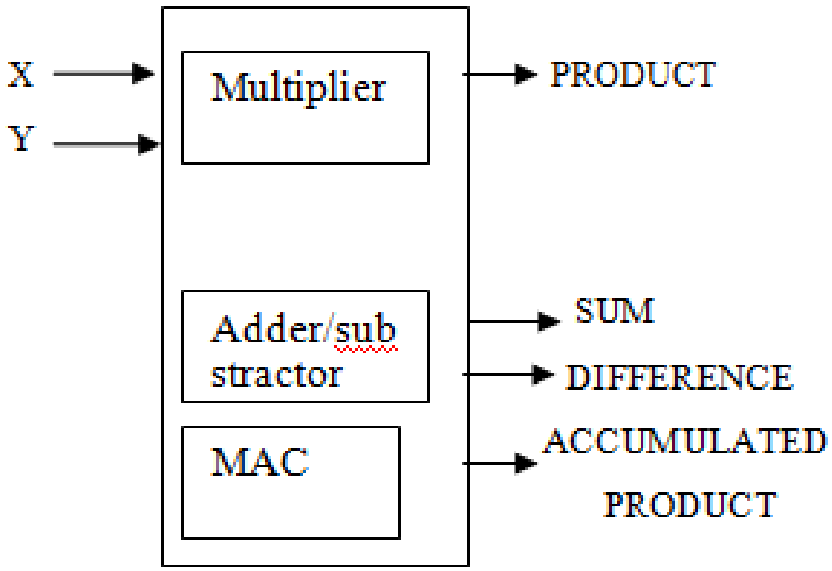


Fig no 4.2 block diagram of ALU

International Journal of Advance Research in Science and Engineering
Vol. No.4, Issue No. 12, December 2015
www.ijarse.com
IJARSE
ISSN 2319 - 8354

V. SYNTHESIS RESULTS

The Vedic mathematics is the powerful tool that can optimize the performance of the whole ALU design. The Vedic mathematics will have less number of calculations as compared with the regular mathematics hence the hardware resources are less, hence it will be efficient in area at the same time requires less propagation delay due to the less number of calculations. This leads to fast calculation which makes efficient in power. The ALU design consists of modules like Multiply-Accumulate unit and adder/sub tractor. The Mac is main module that consists of adder and multiplier. The 64 bit multiplier designed with Verilog HDL. The RTL design is simulated in Xilinx ISE 13.2i. The modules synthesis reports are presented below

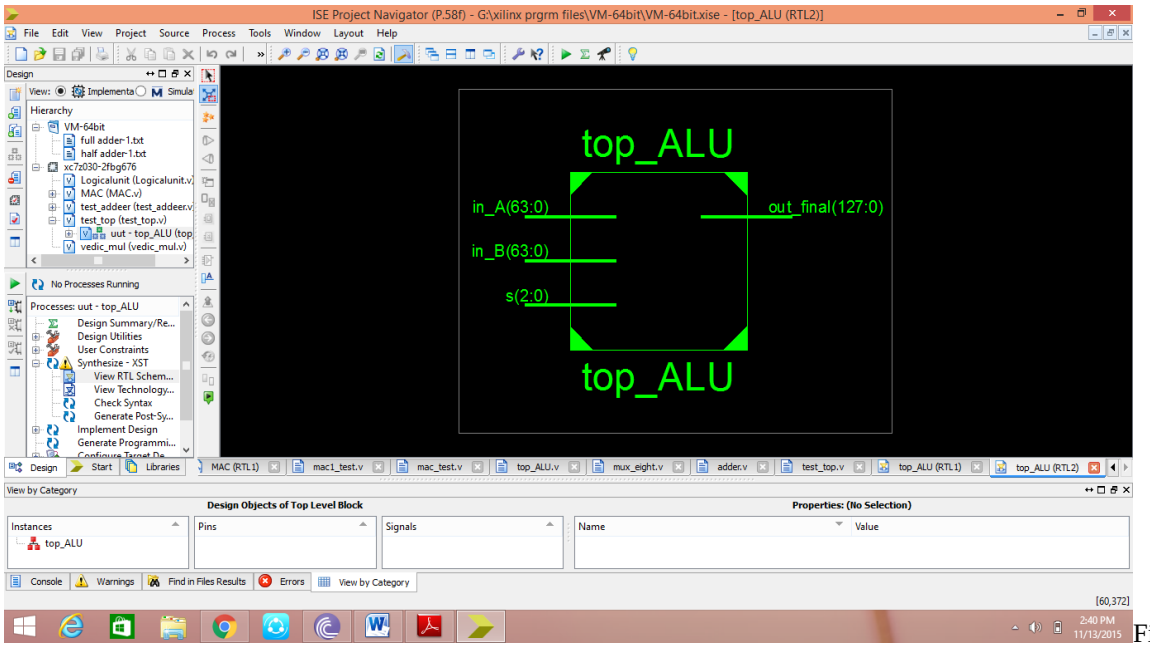


Fig5.1

Top level schematic of ALU

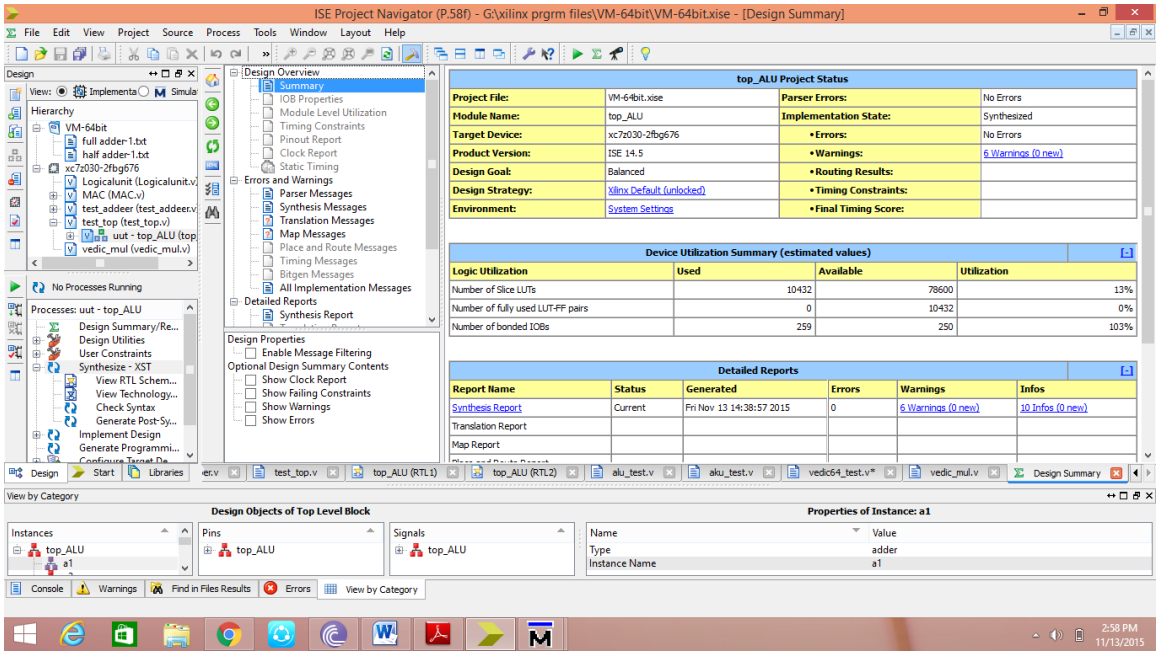


Fig 5.2 Synthesis area report of ALU

International Journal of Advance Research in Science and Engineering
Vol. No.4, Issue No. 12, December 2015
www.ijarse.com
IJARSE
ISSN 2319 - 8354

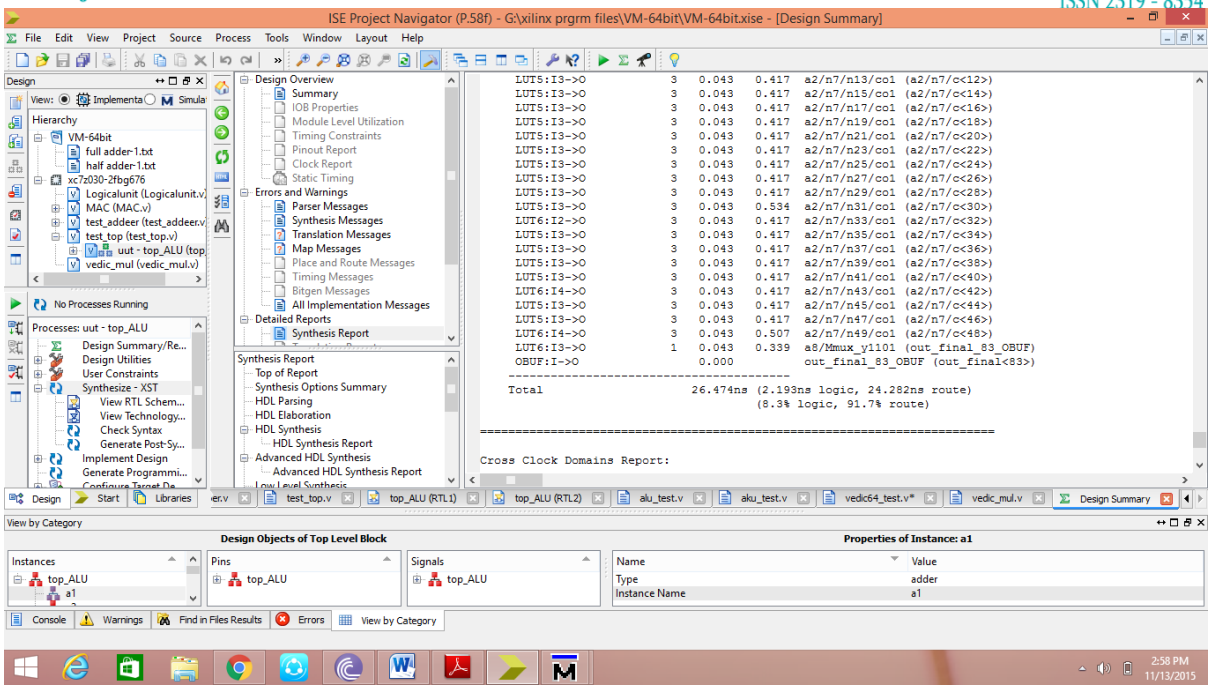
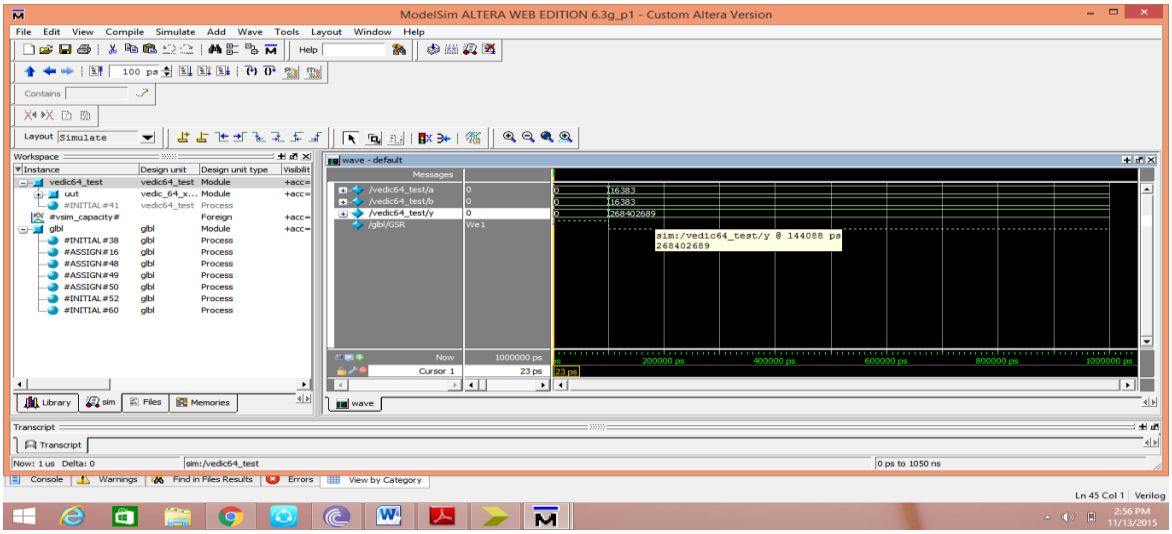


Fig 5.3 Synthesis timing report of ALU

5.1 Simulation Reports

To check the behavior of the multiplier and ALU we have given inputs A, B are the inputs and, multiplication is selected, the multiplication result is given in wave from, which equal to theoretical value



VI.CONCLUSION

I have designed ALU based on multiplier and air thematic unit based on the Vedic mathematics using Verilog HDL and synthesised in Xilinx ISE 13.2and from the report I found that it has lesser delay and lesser power than modern mathematics based ALU.

REFERENCES

[1]. An IEEE journal on Low power ALU design using ancient Mathematics by Anvesh kumar, NIT Jalandhar, Ashish Raman, NIT Jalandhar.

[2] Swami Bharati Krishna Tirtha, Vedic Mathematics. Delhi: Motilalm Banarsidass Publishers, 1965

[3] Vedic Maths Sutras - Magic Formulae [Online]. Available: http://hinduism.about.com/library/weekly/extra/bl vedicmathsutras. https://Vedic maths.org.

[4] Koren Israel, "Computer Arithmetic Algorithms," 2nd Ed, pp. 141-149, Universities Press, 2001.

[5] L. Sriraman, T.N. Prabakar, "Design and Implementation of Two Variable Multiplier Using KCM and Vedic Mathematics," 1st Int. Conf. on Recent Advances in Information Technology, Dhanbad, India, 2012, IEEE Proc., pp. 782-787.

[6] M. Ramalatha, K. Deena Dayalan, S. Deborah Priya, "High Speed Energy Efficient ALU Design using Vedic Multiplication Techniques," Advances in Computational Tools for Engineering Applications, 2009, IEEEProc., pp 600-603.

[7] Jagadguru Swami Sri Bharati KrisnaTirthaji Maharaja, "Vedic Mathematics: Sixteen Simple Mathematical Formulae from the Veda," pp. 5-45, Motilal Banarasidas Publishers, Delhi, 2009.

[8] Himanshu Thapliyal and M. B. Srinivas, "An efficient method of elliptic curve encryption using Ancient Indian Vedic Mathematics," 48th IEEE Int. Midwest Symp.on Circuits and Systems, 2005, vol. 1, pp. 826-828.

[9] Tiwari, Honey Durga, et al., "Multiplier design based on ancient Indian Vedic Mathematics, "Int. SoC Design Conf., 2008, vol. 2. IEEE Proc., pp. II-65 - II-68.

[10] Hsiao, Shen-Fu, Ming-Roun Jiang, and Jia-SienYeh, "Design of high speed low-power 3-2 counter and 4-2 compressor for fast multipliers," IEEE Electronics Letters, vol. 34, no.4, pp. 341-343, Feb. 1998.

[11] D. Radhakrishnan and A. P. Preethy, "Low power CMOS pass logic 4-2 compressor for high-speed multiplication," Circuits and Systems, Proc. 43rd IEEE Midwest Symp., vol. 3, pp. 1296-1298, 2000.

AUTHOR DETAILS

	**SRIKANTH YELLAMPALLI**, Pursuing M.tech (VLSI) from Nalanda institute of Engineering and Technology (NIET),He completed his Bachelors of Technology from Electronics and communication Engineering. His area of interest includes CMOS analog, CMOS digital and Low power VLSI design
	**J KOTESWARA RAO,** Working as assistant professor in Nalanda Institute of Engineering and Technology (NIET),He completed his Bachelors of Technology from Electronics and communication Engineering. His area of interest includes CMOS digital and Low power VLSI and VLSI system design.