A NEW SIMPLIFIED MULTILEVEL INVERTER TOPOLOGY FOR GRID-CONNECTED APPLICATION

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ABSTRACT

The performance of multilevel inverter is high compared to the classical two level inverters owing to their reduced total harmonic distortion, and lower electromagnetic interference. However the setbacks of multilevel inverter are increased number of power devices, complex PWM and gating circuitry. In this paper, a new multilevel inverter topology, capable of generating large number of levels with fewer number of power switches, gating circuits and power diodes is proposed. In contrast to classical multilevel topologies, the presented topology consequences in reduction of the number of power devices and conduction losses. The proposed topology is asymmetrical, employing isolated dc sources of voltage ratio 4:2:1 (Binary fashion). Staircase control PWM at fundamental frequency is employed for the gating of power switches makes it suitable in applications like flexible alternative current transmission systems (FACTS), renewable energy sources, drives control and vehicle propulsion system. The structure of the proposed inverter is modular and thus best suited for PV applications. Detailed simulation is carried out using MATLAB/SIMULINK platform and simulation results are presented.

Index Terms: Multilevel İnverter; Topology; Total Harmonic Distortion

I. INTRODUCTION

Multilevel converter based power conversion has become more attractive and viable solution for medium and high-power applications. The basic concept of multilevel converter is to synthesize the desired output voltage in small steps of dc voltages as inputs [1]. By increasing the number of dc voltage inputs (levels), the small voltage steps lead to the production of high power quality waveforms, lower harmonic contents, lower voltage ratings of devices, lower switching losses, and also reduction of (dv / dt) stresses on the load and EMC [2], [3]. In general multilevel converter are categorized into three types, which are cascade converter with isolated dc sources [4], the flying capacitor converter [5] and the diode-clamped converter [6]. The cascaded converter consists of series connected H-bridges for generation of stepped waveforms and as the number of levels increases, the number of H-bridges also increases. The conventional cascade converter can have either symmetric or asymmetric structure. In symmetric structure, the values of all the dc voltage sources are the same. However, the values of dc sources in asymmetric structure are not-equal [7]. The flying capacitor converter uses more number of capacitors for higher levels is a big problem [8]. The number of clamping diodes required are more for higher voltage levels makes the diode clamped converter more complex [9]. New multilevel inverter structure's has been introduced which requires less number of switches in comparison with conventional topology [10].

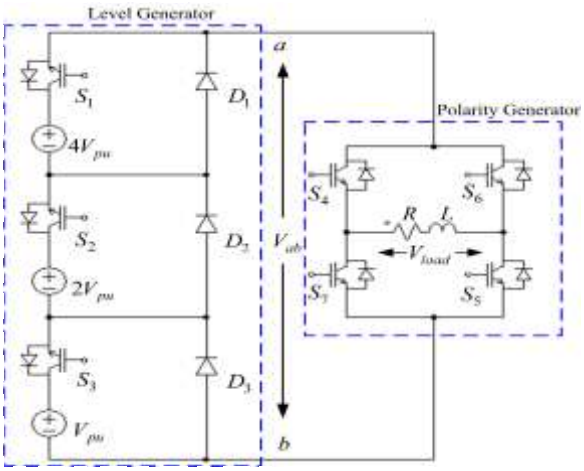


Fig.1 Proposed 15-level Asymmetrical Inverter

In this paper, a new asymmetrical multilevel inverter topology with reduced semiconductor power devices is proposed. The inverter is controlled by fundamental switching PWM as it results in reduced conduction and switching losses. The switching angles are computed using staircase control technique [7] to generate high quality waveform with reduced harmonic content. The operating principle and switching functions are discussed. The simulation results demonstrating the validity of the proposed converter topology with DC voltage ratio 4:2:1 are presented.

II. TOPOLOGICAL DESCRIPTION AND PRINCIPLE OF OPERATION

Fig. 1 shows the structure of the proposed fifteen level asymmetrical inverter topology. In conventional multilevel inverters, the power devices are operated to produce a high-frequency waveform in both half cycle of the fundamental output waveform. However there is no need to use all the power devices in the generation of bipolar output voltage. This is the basic idea that has been devices and incorporated by the proposed topology. The proposed topology consists of two sections namely level generator which is responsible for the generation of stepped voltage waveform and secondly the polarity generator stage which is responsible for generating the polarity of the output voltage. Proper switching of the inverter can produce 15 output voltage levels: 0, 1, 2, 3, 4, 5, 6, -1, -2, -3, -4, -5, -6 V_{pu}. In order to generate 15 levels of output voltage, the voltages of different DC sources must be added, as the output voltage is the sum of the DC voltage sources. Switches S_1, S_2, S_3 are involved in generation of positive levels only and the inversion of polarity is performed by the switches $S_4 - S_6$.

The proposed inverter's operation can be divided into eight switching states, as shown in Fig. 2(A)–(H).The required output positive voltage levels produced by the level generator are generated as follows:

1) MODE 0: Switches S_4, S_6 are ON which short circuits the load terminals resulting in the generation of zero voltage across load. This mode of operation is termed as MODE 0 and the active switches in the current path is shown in Fig. 2(A).
2) MODE 1: Switch S_3 is ON connecting the terminal a to V_{pu} source and terminal b to ground resulting in the generation of voltage $V_{ab} = V_{pu}$. This mode of operation is termed as MODE 1 and the active switches in the current path is shown in Fig. 2(B).

3) MODE 2: Switch S_2 is ON connecting the terminal a to $2V_{pu}$ source and terminal b to ground resulting in the generation of voltage $V_{ab} = 2V_{pu}$. This mode of operation is termed as MODE 2 and the active switches in the current path is shown in Fig. 2(C).
4) MODE 3: Switch S_1, S_2 is ON connecting the terminal a to $3V_{pu}$ (sum of $1V_{pu}$ and $2V_{pu}$) and terminal b to ground resulting in the generation of voltage $V_{ab} = 3V_{pu}$. This mode of operation is termed as MODE 3 and the active switches in the current path is shown in Fig. 2(D).
5) MODE 4: Switch S_1 is ON connecting the terminal a to $4V_{pu}$ source and terminal b to ground resulting in the generation of voltage $V_{ab} = 4V_{pu}$. This mode of operation is termed as MODE 4 and the active switches in the current path is shown in Fig. 2(E).
6) MODE 5: Switch S_1, S_3 is ON connecting the terminal a to $5V_{pu}$ (sum of $1V_{pu}$ and $4V_{pu}$) and terminal b to ground resulting in the generation of voltage $V_{ab} = 5V_{pu}$. This mode of operation is termed as MODE 5 and the active switches in the current path is shown in Fig. 2(F).
7) MODE 6: Switch S_1, S_2 is ON connecting the terminal a to $6V_{pu}$ (sum of $2V_{pu}$ and $4V_{pu}$) and terminal b to ground resulting in the generation of voltage $V_{ab} = 6V_{pu}$. This mode of operation is termed as MODE 6 and the active switches in the current path is shown in Fig. 2(G).
8) MODE 7: Switch S_1, S_2, S_3 is ON connecting the terminal a to $7V_{pu}$ (sum of $1V_{pu}$, $2V_{pu}$ and $4V_{pu}$) and terminal b to ground resulting in the generation of voltage $V_{ab} = 7V_{pu}$. This mode of operation is termed as MODE 7 and the active switches in the current path is shown in Fig. 2(H).

Table.1 Switching Sequences for Each Level

V_{pu}	Switching patterns	V_{pu}	Switching patterns
7	S_1, S_2, S_3, S_4, S_5	-7	S_1, S_2, S_3, S_6, S_7
6	S_1, S_2, S_4, S_5	-6	S_1, S_2, S_6, S_7
5	S_1, S_3, S_4, S_5	-5	S_1, S_3, S_6, S_7
4	S_1, S_4, S_5	-4	S_1, S_6, S_7
3	S_2, S_3, S_4, S_5	-3	S_2, S_3, S_6, S_7
2	S_2, S_4, S_5	-2	S_2, S_6, S_7
1	S_3, S_4, S_5	-1	S_3, S_6, S_7
0	S_4, S_6	0	S_4, S_6

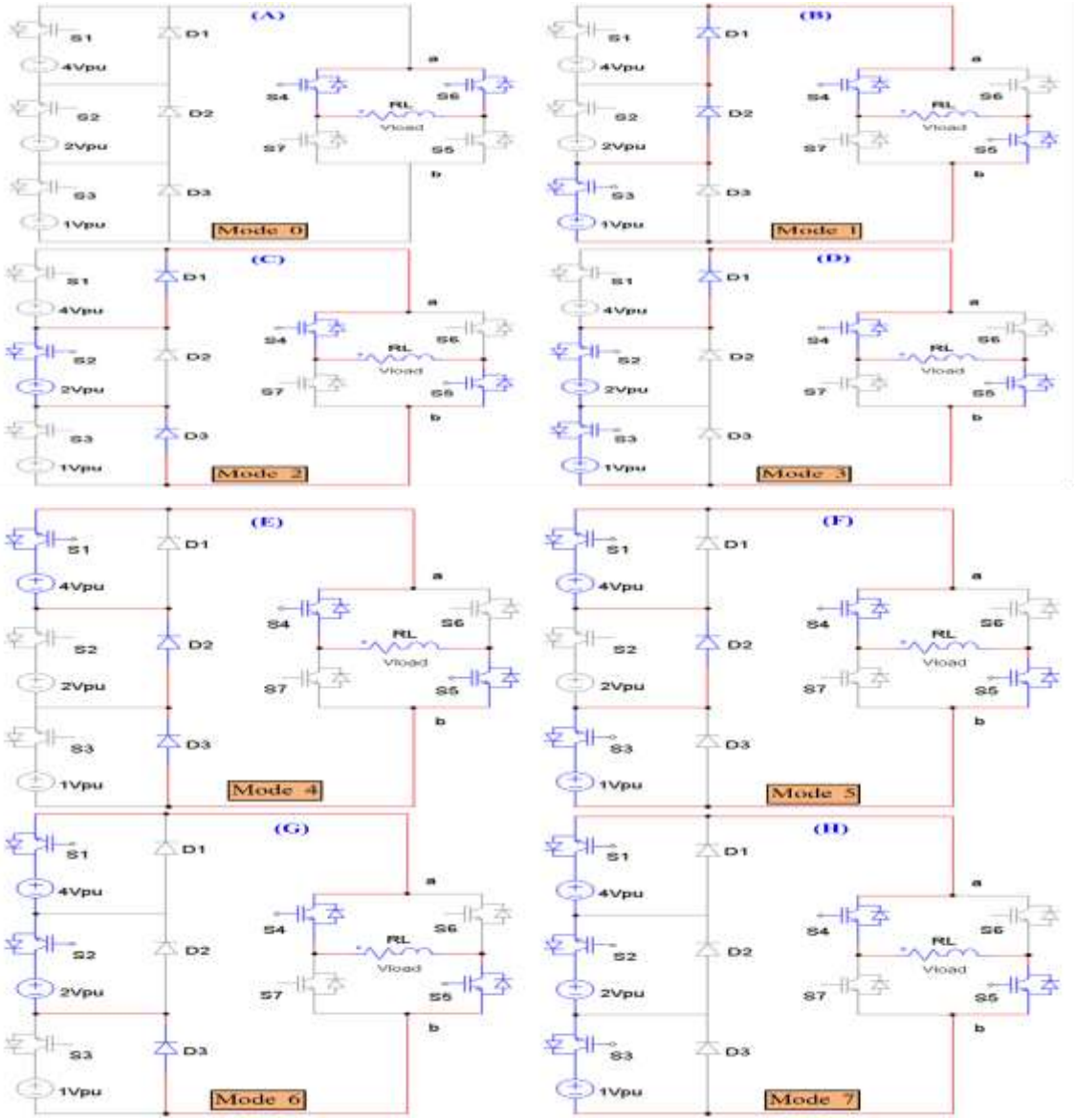


Fig.2 Operating Modes of the Inverter

In Table I, the switching patterns required for the generation of desired voltage level is tabulated. The structure of the proposed inverter can also be applied for three-phase applications with the same principle. As this topology uses isolated dc supplies, it does not have voltage-balancing problems due to fixed input dc voltage values. In comparison with a conventional cascade topology, it requires just one-third of isolated power supplies. Fig. 3 shows the structure of the three phase inverter with the proposed basic topology.

According to Fig. 3, the multilevel positive voltage is fed to the full-bridge inverter for polarity generation. It requires fewer components in comparison to conventional inverters.

III. STAIRCASE PWM SCHEME

There are many PWM schemes for inverter control such as multi carrier SPWM with phase disposition (PD), Alternative phase opposite disposition (APOD), Phase opposition disposition (POD), and space vector PWM (SVPWM). In the proposed topology, to synthesize the 15-level output voltage waveform, prior calculation of switching angles is done according to the switching patterns from Table 1. The inverter is switched at fundamental frequency (50 Hz). The staircase PWM requires only one sinusoidal reference wave, of which only

seven regions are needed to calculate the switching angles. Fig. 4 shows the stepped-voltage waveform consisting of the output of the proposed inverter with switching angles of triggering signals, which are θ_1 to θ_7. Due to quarter wave symmetry only these seven angles needs to be calculated.

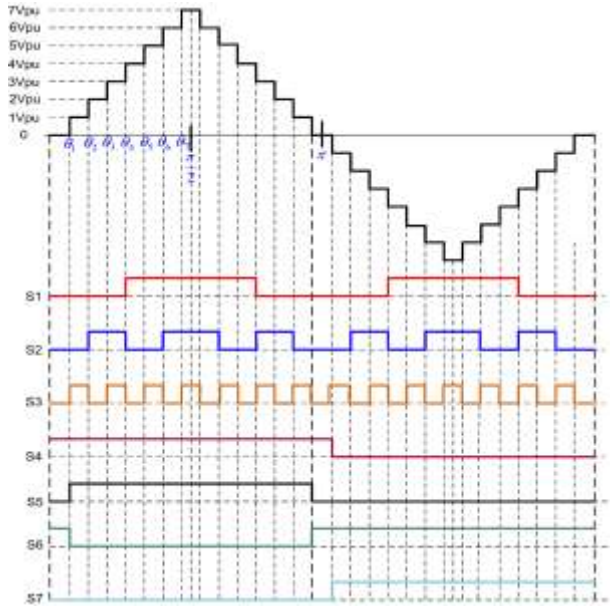


Fig.3 Stepped-Voltage Waveform with Switching Angles for Power Switches

The switching angles are calculated such that harmonic distortion in the output voltage waveform is minimum.

$$v_o = \sum_{n=1,3,5...}^{\infty} B_n \sin(n\omega t) \qquad (1)$$

The switching angles calculated in advance is given by

$$\theta_n = \sin^{-1}\left(M \times \frac{n-1}{m}\right) \qquad (2)$$

where n is the number of the switching angles, m is the maximum number of switching angles, and M is the modulation index. By controlling the modulation index the output RMS voltage is varied. As M changes the number of output levels remains same with not much increase in the THD. Equation (2) is modified by adding the term k for making the output voltage to track sinusoidal modulating wave.

$$\theta_n = \sin^{-1}\left(\frac{n-1+k}{m+k}\right) \qquad (3)$$

The THD of the output voltage is given by

$$THD = \frac{1}{V_1}\sqrt{\sum_{h=3,5,7...}^{\infty} V_h^2} \qquad (4)$$

where V_1 is the fundamental output voltage peak of the inverter and V_h is the harmonic voltage given as

$$V_1 = \frac{4V_{dc}}{\pi}\left(\cos(\theta_1) + \cos(\theta_2) + \cos(\theta_3) + ... + \cos(\theta_7)\right) \qquad (5)$$

$$V_h = \sum_{h=3,5,7..}^{\infty} \frac{4V_{dc}}{\pi}\begin{pmatrix}\cos(h\theta_1)+\cos(h\theta_2)+\cos(h\theta_3)+.....\\ +\cos(h\theta_7)\end{pmatrix} (6)$$

The switching angles are calculated for a given k using equation (3) and then the fundamental voltage V_1 and harmonic voltage V_h are calculated using equation (5) and equation (6) respectively to compute THD. MATLAB was used to do all the above said calculations using all the equations. Fig. 5 shows the variation of modulation index M (shown as $M(k)$) versus coefficient k.

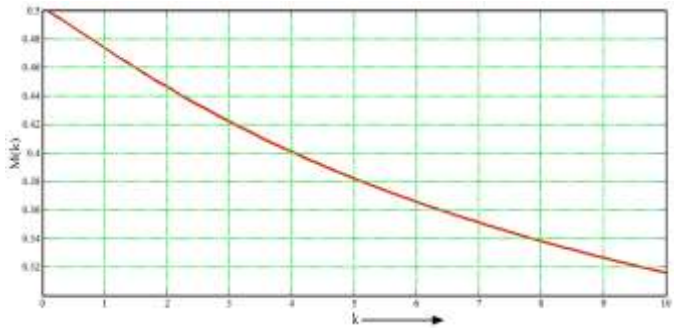


Fig.4 Modulation Index Versus Coefficient k.

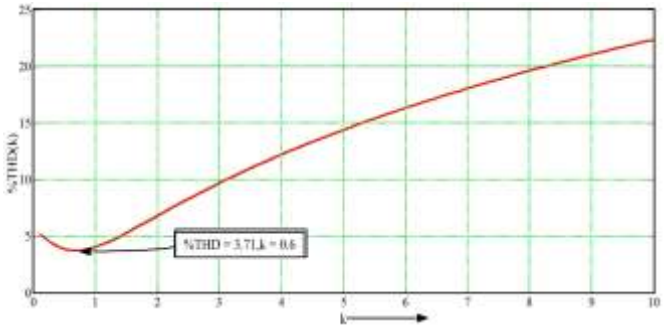


Fig.5 THD of the Output Voltage Versus Coefficient k within 75th Harmonic

It can be seen from the above figure that the modulation index decreases linearly coefficient k increases from 0 to 10. Thus the modulation index and hence the output fundamental voltage can be controlled by adjusting k. The profile of the output voltage THD versus coefficient k is shown in Fig. 6. For k =0 and k =0.6 the THD values are 5.1% and 3.71% respectively which shows that by adding k there is reduction of 1.39% in the THD. Although the difference is small, the latter value of THD satisfies the norms of IEEE standards [15]. As coefficient k increases the M decreases but still the number of output voltage remains same with increasing THD.

The control switching algorithm for generation of gating pulses for all the power switches is shown in Fig. 7. The reference sinusoidal waveform (V_{ref}) is of fixed amplitude and frequency. Once the switching angles are computed according to the value of fundamental voltage required then the switching logic controller generates the gating signals. The logic functions derived for the generation of pulses is given as

$$S_1 = \{1 \Rightarrow (V_{ref} > \sin\theta_4)$$

$$S_2 = \{1 \Rightarrow ((V_{ref} > \sin\theta_1) * (V_{ref} < \sin\theta_4)) + (V_{ref} > \sin\theta_6)$$

$$S_3 = \{1 \Rightarrow ((V_{ref} > \sin\theta_1) * (V_{ref} < \sin\theta_2)) + ((V_{ref} > \sin\theta_3) * (V_{ref} < \sin\theta_4))$$
$$+ ((V_{ref} > \sin\theta_5) * (V_{ref} < \sin\theta_6)) + (V_{ref} < \sin\theta_7)$$

$$S_4 = \{1 \Rightarrow (V_{ref} > 0)$$

$$S_5 = \{1 \Rightarrow (V_{ref} > \sin\theta_1)$$

$$S_6 = \bar{S}_5$$

$$S_7 = \bar{S}_4$$

The topology structure of the proposed inverter requires less number of power devices in comparison to conventional inverters for generation of same voltage levels and Table 2 shows the comparative requirement. It can be inferred from the Table 2 that the number of components of the proposed topology is lower than that of other topologies.

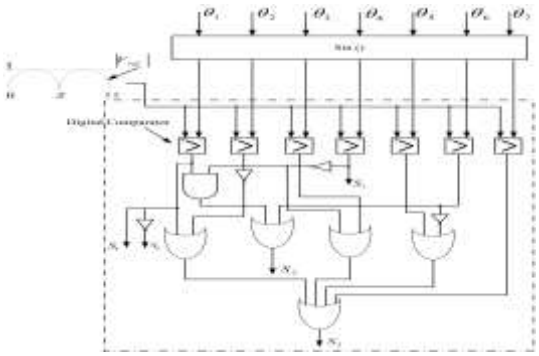


Fig.6 Switching Control Circuit

Table.2 Comparison of the Proposed 15-level Inverter with the Conventional 15-level Inverters on the Basis of Circuit Component Requirements

Inverter Type	Proposed inverter	Diode clamped inverter	Cascaded inverter [7]	Flying capacitor inverter
Main switches	**7**	12	12	12
Main Diodes	**3**	12	0	0
DC voltages	**3**	1	3	1
Balancing capacitors	**0**	0	0	12

IV. SIMULATION RESULTS

To demonstrate the effectiveness of the proposed inverter topology, simulation is carried out in MATLAB/SIMULINK. The inverter dc voltage sources are assigned with magnitude of 25V, 50V and 100V satisfying the ration 1:2:4 in a binary fashion. Simulation is carried out for two cases

Case I: In this case the gating pulses for inverter is generated by simply considering all the switching angles to be $\theta_1 = \theta_2 = \theta_3 = \theta_4 = \theta_5 = \theta_6 = \theta_7 = 12.85^0$. With this scheme the inverter output waveforms for R and R-L

load are presented. The output voltage and current waveform of the proposed inverter feeding R-Load of 100Ω is shown in Fig. 7. The THD is found to be 6.67% in both voltage and current since it is a resistive load. With the same switching control the inverter feeding the R-L Load of 100 Ω and 50 mH is considered and the corresponding waveform is shown in Fig.8.

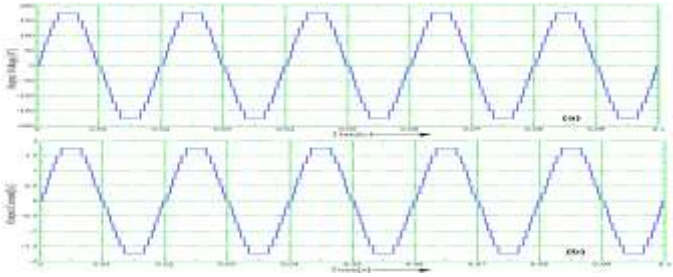


Fig.7 (a) Output Voltage (b) Output Current of the Proposed Inverter Feeding R-Load

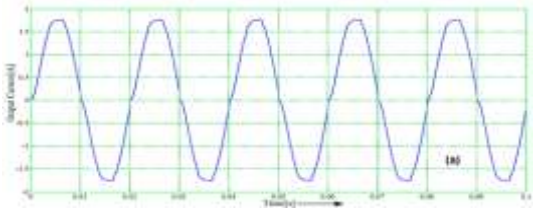
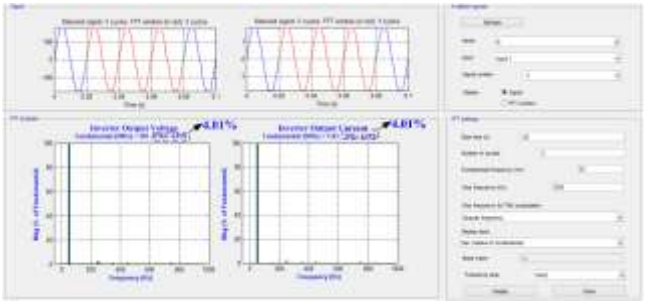


Fig.8 Output Current Fed to R-L load.

Case II: For the second case the gate pulses are generated considering the switching angles and the logic function derived from staircase PWM scheme. Fig. 9 shows the output voltage and current waveforms of the inverter feeding same value of R-Load. The spectrum waveform for voltage and current in Fig. 10 reveals the reduction of THD from 6.67% to 4.01% as per the analysis due to the application of staircase PWM scheme.

Inverter feeding the R-L Load of 100Ω and 50mH is considered and the corresponding waveform is shown in Fig. 11. The spectrum of the output current is shown in Fig. 8(b) which has reduced THD. The proposed inverter topology can be extended to three phase and the corresponding waveforms is shown in Fig. 14. As the number of levels and phase increases the components requires reduces drastically improving the efficiency and reliability of the proposed inverter.



V. CONCLUSION

A hybrid 15-level inverter topology with staircase PWM is proposed. The proposed inverter topology has superior features over conventional topologies in terms of the required power devices and, control requirements, cost, reliability and results in the output voltage near to sinusoidal waveform. It fits suitable for inverters used in power applications such as FACTS, PV systems, UPS. The switching operation is divided into level generation and polarity generation, which add up to the efficiency of the inverter. The staircase PWM employed resulted in

the generation of voltage with THD of 4.24% which complies with the IEEE norms. The detailed simulation results confirm the effectiveness and feasibility of the proposed converter for multilevel dc-ac operation.

REFERENCES

[1]. Chiasson, J.N., Tolbert, L.M., McKenzie, K., Du, J.Z.: 'Control of multilevel converter using resultant theory', IEEE Trans. Control Syst. Tech., 2003, 3, (11), pp. 345–354.

[2]. P. Zhiguo, F.Z. Peng, Harmonics optimization of the voltage balancing control for multilevel converter/inverter systems, in: Proceedings of the IEEE 39th Annual Industry Applications Conference, vol. 4, 3–7 October, 2004, pp. 2194–2201.

[3]. J. Chiasson, L. Tolbert, K. McKenzie, Z. Du, Real-time computer control of a multilevel converter using the mathematical theory of resultants, Elsevier J. Math. Comput. Simul. 63 (3–5) (2003) 197–208.

[4]. J. S. Lai and F. Z. Peng, "Multilevel converters–A new breed of power converters," IEEE Trans. Ind. Applicat., vol. 32, pp. 509–517, May/June. 1996.

[5]. T. A. Meynard and H. Foch, "Multi-level choppers for high voltage applications," Eur. Power Electron. Drives J., vol. 2, no. 1, p. 41, Mar.1992.

[6]. A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point clamped PWM inverter," IEEE Trans. Ind. Applicat., vol. IA-17, pp. 518–523, Sept./Oct. 1981.

[7]. Z. Sang, C. Mao, and D. Wang, "Staircase Control of Hybrid Cascaded Multi-level Inverter", Electric Power Components and Systems, vol. 42, no. 1, pp-23-34, Dec. 2013.

[8]. R. Stala, "Application of balancing circuit for dc-link voltages balance in a single-phase diode-clamped inverter with two threelevel legs," IEEE Trans. Ind. Electron., vol. 58, no. 9, pp. 4185- 4195, Sep. 2011.

[9]. Kangarlu, M.F., Babaei, E., Laali, S.: 'Symmetric multilevel inverter with reduced components based on non-insulated dc voltage sources', IET Power Electron., 2012, 5, (5), pp. 571–581.

[10]. Babaei, E.: 'A cascade multilevel converter topology with reduced number of switches', IEEE Trans. Power Electron., 2008, 23, (6), pp. 2657–2664.