POWER MINIMIZATION TECHNIQUE FOR CIRCUIT UNDER TEST

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ABSTRACT

In this paper, the technique has been presented to minimize the power consumption during testing of a Circuit Under Test (CUT). In proposed scheme a linear feedback shift register (LFSR) is proposed technique which focuses to minimize the power consumption from within Built-in Self-test (BIST) itself. With the help of this technique we can minimize the power consumption during testing of a Circuit Under Test (CUT) in two steps. In the First step, Control Logic (CL) constitutes the clocks of the switching units of the register deactivate for a time frame when output from them is going to be same as previous one and thus minimizing undesired switching of the flip-flops. In the second step, the LFSR reorders the test vectors by interchanging the bit with its next and closest neighbour bit. It retains the fault coverage capability of the vectors unaffected but minimizes the Total Hamming Distance (THD). Therefore there is minimization in power while shifting operation.

Keywords : Built-in Self-test, Control Logic, Fault Coverage, Linear Feedback Shift Register, Total Hamming Distance.

I. INTRODUCTION

Power consumption has become an extensive design consideration in many application areas. Power consumption is also one of the most critical considerations in designing a VLSI system. The main requirement for considering power during test is that power consumption is higher in test mode than in normal mode. Power consumption of a system in test mode is more than that in normal mode because a important correlation occurs between the consecutive test vectors applied during the circuit's normal mode of operation, but this may not be certainly correct for applied test vectors in test mode of operation. Low correlation among the test vectors increases switching activity and causes power consumption in the circuit.

Popular approach for low power testing is BIST as it contributes more scope for low power techniques to be used. BIST uses an LFSR as test pattern generator (TPG) and LFSR produces all possible test vectors with the proper use of tap sequence. The pseudorandom behaviour of the LFSR minimizes the correlation among test vectors therefore it can acquire high fault coverage in a relatively short run of test vectors. The lack of correlation among test vectors significantly increases the hamming distance among the vectors which causes increased switching activity in the CUT. Generally this causes more power consumption in the test mode of operation. Therefore it is required to realize the most appropriate linear

feedback shift register which is in itself is power efficient and the test vectors produced are also power efficient. Therefore they cause minimum switching activity when scanned in into a scan chain of CUT, without compromising the fault coverage.

II. PROLOGUE

Many low power testing techniques have been proposed. Several categories of low power testing techniques can be found. The External Testing techniques include the methodologies based on Automatic Test Pattern Generator (ATPG), Vector Reordering. ATPG algorithms can broadly be classified into random and deterministic algorithms. Random ATPG algorithms involve generation of random vectors and test efficiency *(* test quality quantified by fault coverage) is determined by fault simulation. Deterministic ATPG algorithms generate tests by processing a structural netlist at the logic level of abstraction using a specified fault list from a fault universe.

A new version of the path-oriented, decision-making (PODEM) algorithm is proposed where the clever assignment of don't-care bits minimizes the number of transitions that occur in the CUT between two consecutive test vectors. Architecture whereas the BIST include techniques based on LFSR, Test Scheduling, Circuit Partitioning and Reseeding.

The vector ordering can be used in BIST environment as well. In ordering techniques, the THD i.e. the sum of the hamming distances is minimized by modifying the order in which test vectors of a given test sequence are shifted into the CUT. The Travelling Salesman Algorithm (TSA) has been quite useful for ordering the test vectors. The test vector ordering has been useful in minimizing the hamming distance among test vectors and thereby reducing in average and peak power [2] [7]. Reordering of test vectors does not affect the fault coverage as overall the same set of test vectors are applied, just their order is modified [6].

Two methods used for reordering of test vectors in order to reduce the dynamic power dissipation during testing of combinational circuits. Two search methods, 2-opt heuristic and a genetic algorithm based approach has applied and results obtained for combinational circuits. These techniques can be applied during external testing or deterministic BIST as well.

III. MOTIVATION

From the following studies motivation for the proposed work emerges. The available literature emphasis upon ordering the test vectors after obtaining the test vector sequences form the LFSR and the LFSR can itself be power efficient if redesigned for the purpose. The main purpose of the work is to design a LFSR which in itself is power efficient and the test vectors produced from it are also power efficient. Therefore, the test vectors induce lower switching when scanned in.

IV. PROPOSED METHODOLOGY

In the proposed technique, LFSR has been designed such that it reorders the test vectors to reduce the switching activity and consumes little power as compared to conventional LFSR. The switching unit (flip-flops) of the LFSR toggle unnecessarily in the process of generating 2^n sequence when same bits are repeated for a particular set of test sequences. Therefore the non

performing flip - flops are deactivated for particular time frame. The flip - flops are deactivated by maintaining the clock signal to state '0' [10].

The behaviour of the switching unit is projected in the Table 1 [10] [12].

Table 1 TRUTH TABLE FOR THE MODIFIED CLOCK

Data_in	Data_ out	Clock	Modified Clock
1	0	1	1
0	1	1	1
1	1	1	0
0	0	1	0

The truth table logic can be realized by the use of an XOR and an AND gate as shown in the Fig.1 [12].

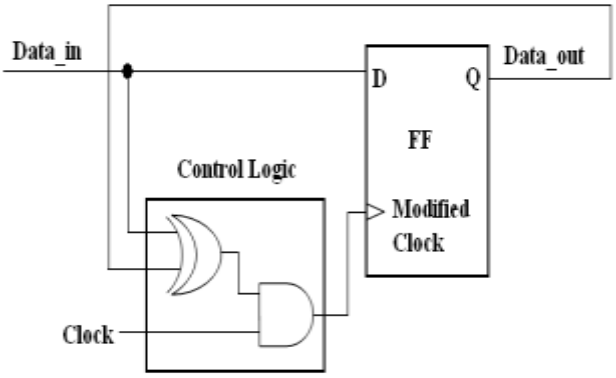

Figure1: Switching unit of LFSR with Modified Clock

The CL logic shown in Fig. 1 can be used with each LFSR cell without modifying its tap sequence and thus without changing its behaviour. Thus the clock signal is modified in order to minimize power consumption. The THD is measure of changes occurring among the test vectors. These changes determine the amount of switching activity in a CUT. The THD can be minimized if test vectors are shifted in proper order. The LFSR with control logic is used along with a reordering algorithm based on bit interchanging method in [2]. In an n-bit LFSR with bits 1, 2, 3, 4…q, q+1, n, if the bit n (the selection bit) has a value '0' (or '1') the interchanging is performed between bit 1 & bit 2, between bit 3 & bit 4 and so on. If bit n has a value of 1 (or 0) then no interchanging is performed. This process produces a new order of test vectors. Now it can be explain with this example. Therefore we take a set of test vectors produced from a maximal length 3-bit LFSR. Applying the bit interchanging methodology a new order of the same test vectors is acquired. The effective reduction in the hamming distance is represented in Table 2 [10] [11].

Table 2 TOTAL HAMMING DISTANCE REDUCTION FOR 3-BIT LFSR

Test Vectors	Test vectors from Conventional LFSR	Reordered Test Vectors
V1	011	101
V2	001	001
V3	100	100
V4	010	010
V5	101	011
V6	110	110
V7	111	111
THD	11	9
New order of test vectors: V5 → V2 → V3 → V4 → V1 → V6 → V7		

V. PROPOSED ARCHITECTURE

Based on the suggested bit interchanging methodology, the modified LFSR can be designed using the conventional LFSR and a group of two-input multiplexers where bit n is considered as the selection line of the multiplexers. The architecture for interchanging the bits as per the proposed methodology is presented in Fig. 2 [10] [12].

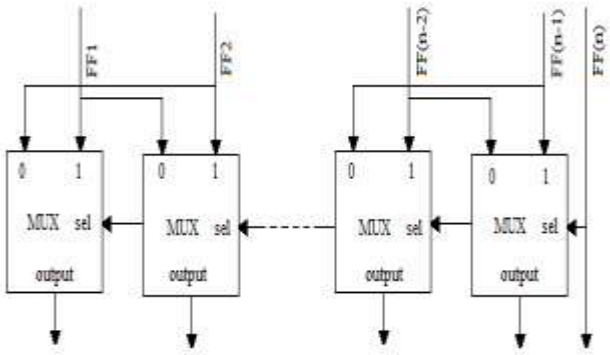

Figure 2: Architecture of Bit Interchanging Module

Integrating the Bit Interchanging Module with the modified clock LFSR makes the design more power efficient as shown in Fig. 3 [12].

The Architecture of 3-Bit modified LFSR in shown in Fig. 3 [12].

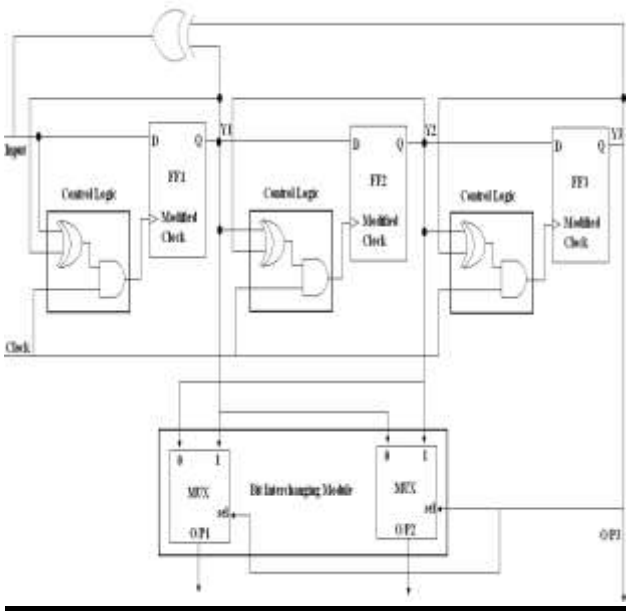

Figure 3: Architecture of 3-Bit Modified LFSR

In this architecture the CL block contains the XOR and AND logic for controlling the clock as shown in Fig. 1. The output from the LFSR is passed to the bit interchanging module which constitutes of multiplexers. It interchanges the bits as per the proposed methodology and finally generates a set of reordered test vectors [12].

VI. EXPERIMENTAL RESULTS AND ANALYSIS

Test vectors are actually the same but their order of scan shifting changes. The Total Hamming Distance (THD) reduction obtained with maximal length 3-bit LFSR is presented in Table 3.

TABLE 3 TOTAL HAMMING DISTANCE REDUCTION

Maximal length LFSR	THD without order	THD with order	THD Reduction (%)
3-bit LFSR	11	9	18.18

Total Power Consumption of 3-bit Conventional LFSR and LFSR with modified clock is presented in Table 4.

TABLE 4 TOTAL POWER CONSUMPTION OF CONVENTIONAL LFSR AND LFSR WITH MODIFIED CLOCK

LFSR Designs	Total power consumption (mW)
Conventional LFSR	22mW
LFSR with modified clock	17mW

VII. CONCLUSION

Testing is the most important issue in the development process of an integrated circuit. The issues that center on test are manufacturing yield, product quality and test cost. To address these test issues design-for-testability (DFT) techniques are used. A method which effectively minimizes the average power consumption due to test application has been proposed. Proposes two architectures to apply them to the circuit under test. Techniques available focused upon minimizing the switching activity from the test patterns generated from the generator. The switching activity minimizing techniques with a power efficient test pattern generator will be a good step. Therefore a modification is proposed in the conventional LFSR by integrating it with control logic module and bit interchanging module. This culminates into a novel

architecture of the test pattern generator (TPG). The modified TPG architecture is efficient of not only deactivating the switching units for a particular time period but also reorders the test vectors to minimize the transition activity. The advantage of this proposed TPG is that it can be used with any other low power technique to have further minimization in power. It is worthwhile to note that our architecture can be easily integrated into an existing design flow, and does not affect the efficiency of the BIST architecture, since it saves power with high fault coverage.

Note: The Power Consumption with modified LFSR is 17mW. So power saving is about 22% then the conventional LFSR.

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