COMPARATIVE ANALYSIS OF POWER REDUCTION IN SRAM 6T AND 4T

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ABSTRACT

Static Random Access Memory (SRAM) to be one of the most fundamental and vitally important memory technologies today. Because they are fast, robust, and easily manufactured in standard logic processes, they are nearly universally found on the same die with microcontrollers and microprocessors. Due to their higher speed SRAM based Cache memories and System-on-chips are commonly used. Memories are an integral part of most of the digital devices and hence reducing power consumption of memories as well as area reduction is very important as of today to improve system performance, efficiency and reliability. Most of the embedded and portable devices use SRAM cells because of their ease of use as well as low standby leakage.

Keywords: Static Random Access Memory, DSTN, Cmos Technology, Dynamic Voltage Scaling, Static Noise Margin

I. INTRODUCTION

The scaling of CMOS technology has significant impacts on SRAM cell random fluctuation of electrical characteristics and substantial leakage current. Exponential increase in VLSI fabrication process has resulted in the increase of the densities of Integrated Circuits by decreasing the device geometries. But devices with such high densities are susceptible to high power consumption and run time failures. Apart from such concerns, other factors such as a growing class of portable devices like PDA, cellular phones, portable multimedia devices etc have given designers a motivation to look into low power design and today, not only device geometries are a technology focus, but also reducing the existing topologies keeping the functionality intact is also a major area. Recent surveys indicate that roughly 30 % of the worldwide semiconductor business is due to memory chips. Over the years, technology advances have been driven by memory designs of higher and higher density. Circuit designers usually state memory capacities in terms of bytes (8 bits); each byte represents a single alphanumeric character. Very large scientific computing systems often have memory capacity stated in terms of words (32 to 128 bits). Each byte or word is stored in a particular location that is identified by a unique numeric address. Due to device scaling there are several design challenges for nanometer SRAM design. A SRAM cell must meet the requirements for the operation in submicron/nano ranges.

1.1 Static Random Access Memory (SRAM) operation

It consists of two cross-coupled inverters and two access transistors. The access transistors are connected to the word line at their respective gate terminals, and the bit lines at their source/drain terminals. The word line is used to select the cell while the bit lines are used to perform read or write operations on the cell. Internally, the cell holds the stored value on one side and its complement on the other side. For reference purposes, assume that node q holds the stored value while node holds its complement. The two complementary bit lines are used to improve speed and noise rejection properties.

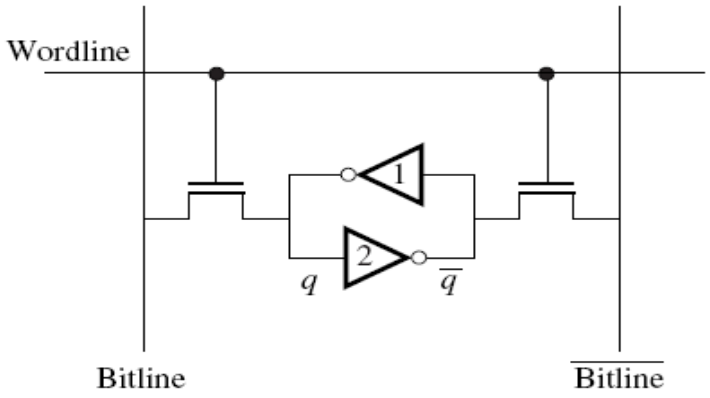

Fig.1 Static Memory Operation

The power consumption is major concern in Very Large Scale Integration (VLSI) circuit design and reduce the power dissipation is challenging job for low power designers. International technology roadmap for semiconductors (ITRS) reports that "leakage power dissipation" may come to dominate total power consumption. The sub-threshold leakage power is the main reason to increase the leakage power. So there are some techniques to reduce this leakage power:-

II. POWER REDUCTION TECHNOLOGY

The power consumption is major concern in Very Large Scale Integration (VLSI) circuit design and reduce the power dissipation is challenging job for low power designers. International technology roadmap for semiconductors (ITRS) reports that "leakage power dissipation" may come to dominate total power consumption. The sub-threshold leakage power is the main reason to increase the leakage power. So there are some techniques to reduce this leakage power:-

- Memory partitioning.
- Sleep stacks technique.
- Adaptive sleep technique.
- Dynamic voltage scaling.
- Quiet bit line architecture.
- Drowsy back bias technique etc.

Power reduction scheme that is tailored for RT and application in a dual-power-supply SRAM is proposed. In order to reduce the active mode power, a BL power calculator (BLPC) is proposed to estimate the BL power for level optimization. Furthermore, a digitally controllable retention circuit (DCRC) is employed to reduce the control power of the standby mode generator. A digitally controllable retention circuit regulates in the standby mode with small control power. These circuits are implemented in a dual-power-supply SRAM in 28-nm CMOS technology.

III. COMPARISION OF SRAM 4T VERSUS 6T

There are various trade-offs between 4T SRAM cells which use four bulk transistors (and have poly resistor or TFT loads) and 6T SRAM cells which use six bulk transistors (and use bulk PMOS loads). 4T SRAM cells have dominated the stand-alone SRAM market since first introduced in the 1970's, but 6T SRAM cells have been dominant for on-chip storage in advanced microprocessors and other logic circuits. However, recently there has been a resurgence of interest in 6T cells for stand alone SRAM applications. While 4T cells are typically smaller, they generally require a more complex process, and have poorer stability, especially at low voltage.

IV. METHODOLOGY USED BY RESEARCHERS

[**Geetika Srivastava, et-al, 2012]** has presented limiting effects technology scaled down on power reduction strategies. The power reduction strategy utilize the property of standby circuit power reduction by reducing voltage swing available to cell by replacing ground and supply nodes by virtual ground and virtual supply nodes respectively. Important precaution to be taken in this method is complete charge removal from virtual nodes before next operation**.** The ever increasing dimension reduction is imposing challenges to cell stability and leakage. Analysis of sub-threshold design has focused on logic design with proper leakage power management. Since SRAM consumes a significant percentage of total area and total power for many digital chips], so it's always a major concern to optimize SRAM in order to improve overall performance of system. The 6T SRAM and its modified versions have been simulated in 32nm, 45nm, 65nm, 90nm and 120nm feature size. The relative leakage power dissipation has been compared for architectures discussed. Sub-threshold SRAM provides great advantage in terms of on-chip memory energy consumption. Conventional 6T SRAM cell alone cannot function in sub threshold as its bit-line leakage put limitation on number of bit-cells on a bit-line. A bit-cell with reduced leakage dissipation in nanometer range solves this problem to greater extent.

[**Budhaditya Majumdar, et-al, 2011]** has presented a novel CMOS 6-transistor SRAM cell for different purposes including low power embedded SRAM applications and stand-alone SRAM applications. In conventional six-transistor (6T) SRAM cell, read stability is very low due to the voltage division between the access and driver transistors during read operation. In existing SRAM topologies of 8T, 9T and higher transistor count, the read static noise margin (SNM) is increased but size of the cell and power consumption increases relatively. Exponential increase in VLSI fabrication process has resulted in the increase of the densities of Integrated Circuits by decreasing the device geometries. Extending this operating scheme also allows us to propose a single bit line design that achieves a relatively smaller area while retaining all of the power saving

advantages. In the proposed technique, the SRAM cell operates by charging/discharging of a single bit-line (BL) during read and write operation, resulting in reduction of dynamic power consumption to only 40% to 60% (best case / worst case) of that of a conventional 6T SRAM cell. The power consumption is further decreased if the switching operational voltage of the bit-line lies between 0.25VDD to 0.5VDD. All simulations are done using 0.18um Technology**.**

[S.S.Rathod, et-al, 2011] has presented Investigation of Stack as a Low Power Design Technique for 6-T SRAM Cell. This paper evaluates SRAM cell with and without introducing stacking in nanometer regime. Overall leakage in a stack of transistors reduces due to modification of gate to source voltage, threshold voltage and drain induced barrier lowering. The self-reverse bias effect can be achieved by turning off a stack of transistors. Turning off more than one transistor in a stack raises the internal voltage (source voltage) of the stack, which acts as reverse biasing the source. The voltages at the internal nodes depend on the input applied to the stack. From various simulations carried out it is found that stack technique helps in the reduction of leakage current that further reduces power consumption and hence it can be used for the design of ultra low power SRAM circuits. Full stack obviously behaves better than the half stack. This reduction of power consumption is at the cost of increased silicon area and propagation delay. Other issues like SNM, increase in stack and variation in length are also discussed.

[Rajani H.P, et-al, 2011] has presented a novel stable SRAM for ultra low power deep submicron cache memories. This paper explores a novel circuit level approach to reduce power in the SRAM cell during active mode of operation as well as standby mode by incorporating NMOS-PMOS pair in each pull down path. Dynamic frequency and voltage scaling (DFVS) and adaptive voltage scaling (AVS) are techniques that reduce voltage or frequency, on the fly. Power gating switches off power to portions of the chip that are not in use. Body biasing or "back biasing" is a leakage reduction technique that uses substrate bias to raise voltage thresholds. Better stability is also reported with large variations in temperature when compared to the standard 6-T SRAM cell and other representative low leakage power SRAM cells due to self controlling feedback. This novel cell achieves excellent active mode power minimization (which is usually not addressed in SRAM designs which achieve standby mode power minimization) along with good leakage power reduction.

[Jae-Ho Ryu, et-al, 2010] has presented a Low-Power Accessless SRAM Macro in Logic CMOS Technology. This paper approached a novel low-power SRAM based on 4-transistor (4T) latch cell is described. The memory cells are composed of two cross-coupled inverters without access transistors. To achieve higher reliability and longer battery life for portable applications, the design of low-power SRAM array is highly desirable. Reducing the swing voltage on the high capacitive signal buses is an effective way to save the operating power. To demonstrate the concept of the proposed SRAM, a 16 kbit SRAM prototype has been designed and fabricated with 0.18 _m logic CMOS technology using microphotograph. In consequence of small voltage swing on high capacitive bitlines, datalines and wordlines, the new SRAM saves 30~40 % of the total active power compared with the conventional 6T SRAM. The measured and simulated results have confirmed that the small-swing 4T SRAM might be effective in realizing low-power embedded memory for mobile applications.

V. SRAM CIRCUITS, PARAMETERS AND RESULTS USED BY RESEARCHERS

Table1: SRAM Circuits, Parameters and Results used by Researchers

S. no.	Solution approaches	Circuit Parameters	Software used	Results
1.	✓ Stacked sleep technique	✓ Vsb= 0v	✓ H spice	✓ Supply voltage =0.9v
	✓ Sleepy keeper technique	✓ Temperature= 70c	H spice	✓ Saving in leakage power.
	✓ adaptive sleep approach	✓ (Vth)=200mV	H spice	✓ It gives best results with high accuracy.
	✓ Full & half Stack tech. for 6T SRAM cell.	✓ Channel length 90-180n	H SPICE	✓ Reduction of power consumption but increased silicon area and delay.
2.	✓ Memory partitioning	✓ Vgs=0	✓ Tanner	✓ Higher accuracy
	✓ Memory organization	✓ High/Low Vt (45 and 32 nano meters)		✓ Reduced SRAM leakage power.
3.	✓ Data-retention voltage technique	✓ DRVmax=190 mv	✓ Tanner	✓ Reduced leakage power when device is idle
	✓ Data voltage scaling	✓ maximum empirical correlation= 3.5%	✓ Tanner	✓ Reduces power per bit by 12-46%.

VI. SIMULATION AND RESULT

Objective: - To design and draw the schematic layout of an inverter. The design specification as given as follows……

VII. INVERTER CIRCUIT OPERATION

Complementary metal-oxide semiconductor (cmos) technology for constructing integrated circuits. CMOS circuits are constructed in such a way that all PMOS must have an input from the voltage source or from another PMOS transistor. Similarly, all NMOS transistors must have either an input from ground or from another NMOS transistor.

The composition of a PMOS transistor creates low resistance between its source and drain contacts when a low gate voltage is applied and high resistance when a high gate voltage is applied. On the other hand, the composition of an NMOS transistor creates high resistance between source and drain when a low gate voltage is

applied and low resistance when a high gate voltage is applied. CMOS accomplishes current reduction by complementing every nMOSFET with a pMOSFET and connecting both gates and both drains together. A high voltage on the gates will cause the nMOSFET to conduct and the pMOSFET to not conduct while a low voltage on the gates causes the reverse. This arrangement greatly reduces power consumption and heat generation. However, during the switching time both MOSFETs conduct briefly as the gate voltage goes from one state to another. This induces a brief spike in power consumption and becomes a serious issue at high frequencies.

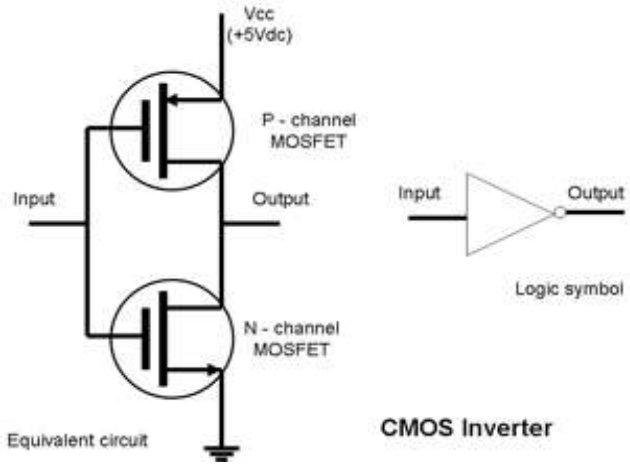

Table2: Inverter circuit parameters

S. No.	Circuit Parameters	Value
1.	Voltage(vin)	5 v
2.	Frequency(f)	5 meg
3.	Width(w)	2.5 u
4.	Length(L)	250n

Inverter module file

```
workspace loadfrom -path .
cell open -design INVERTER -cell Cell0 -type schematic -newwindow
window move -left 224 -top 224 -width 1300 -height 573 -undock -max
window fit -x0 -890 -y0 -1464 -x1 3351 -y1 1133 -units iu
workspace dockinglayout load -file {.\dockinglayout.xml}
source open.design -relativeto user
source open.design -relativeto design
```

Results: - An experiment is performed using TANNER tool. A PMOS and NMOS are connected together by a wire. Both devices are connected and have same input voltage supply

Vdd=5v DC. Frequency applied at the input level power analysis and a 5 volt input pulse for transient analysis is considered for the experimentation. The output waveform is simulated under the process of VTC transient analysis for two different lengths and widths.

Schematic layout design: - This design gives a representation of the elements of a system using abstract, graphics symbols rather than realistic pictures. When designing a layout there are four basic steps;

- Design the schematic in S-EDIT.
- Simulate the schematic to make sure it behaves as you epect using T-SPICE.
- Layout schematic in L-EDIT.
- Perform an LVS schematic.
- Simulate the layout using T-SPICE with a high-level spice model.

Fig.1 shows the basic CMOS inverter which has two transistors of NMOS and PMOS transistor. These two transistors are connected with each other by a wire. Both devices are connected and have same input voltage supply Vdd=5v DC. Input voltage and input frequency is applied at the transistors to calculate the output for two different (W/L) ratios. CMOS circuit layout is described for two same width and length W1= 2.5u, L1= 250n and W2= 2.4u, L2= 250n. With the noise factor NF=1 CMOS inverter realizes the output as high value (1) if we apply the low inputs (0) and gives low output if we apply the high input.

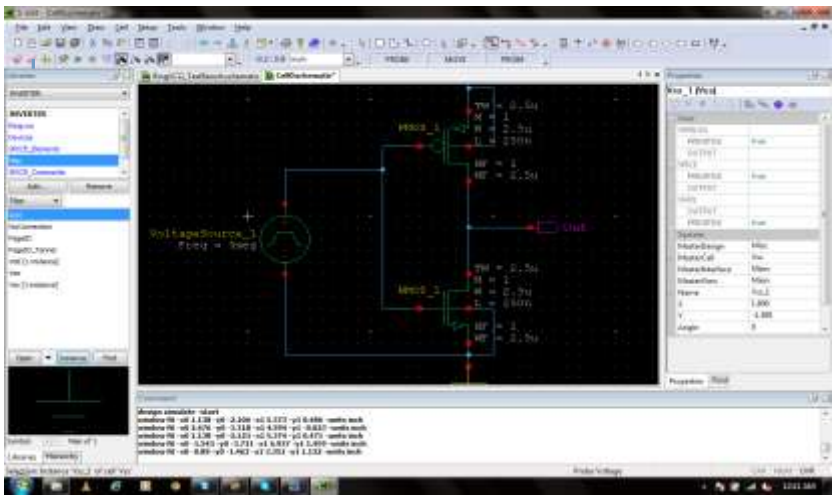

Fig. 1 Schematic layout of an inverter

Fig.2 shows the VTC analysis of an inverter. Voltage Transfer Curve (VTC), which is a plot of input vs. output voltage. From such a graph, device parameters including noise tolerance, gain, and operating logic-levels can be obtained. Ideally, the voltage transfer curve (VTC) appears as an inverted step-function - this would indicate precise switching between *on* and *off* - but in real devices, a gradual transition region exists. The VTC indicates that for low input voltage, the circuit outputs high voltage; for high input, the output tapers off towards 0 volts. The slope of this transition region is a measure of quality - steep (close to -Infinity) slopes yield precise switching. In VTC analysis the input voltage is set to approx 1V. To calculate the noise margin two input voltages are applied to CMOS circuit i.e. lower input voltage V_{IL}= 0.756 and lower output voltage $V_{OL=}$ 0V. Lower input noise margin is given by the difference of lower input voltage and lower output voltage i.e. $NM_L = V_{IL} - V_{OL}$. Higher input noise margin is given by the difference of higher output voltage V_{OH} = 2.5 and lower output voltage V_{OL} = 1.26. $NM_H = V_{OH}-V_{OL.}$

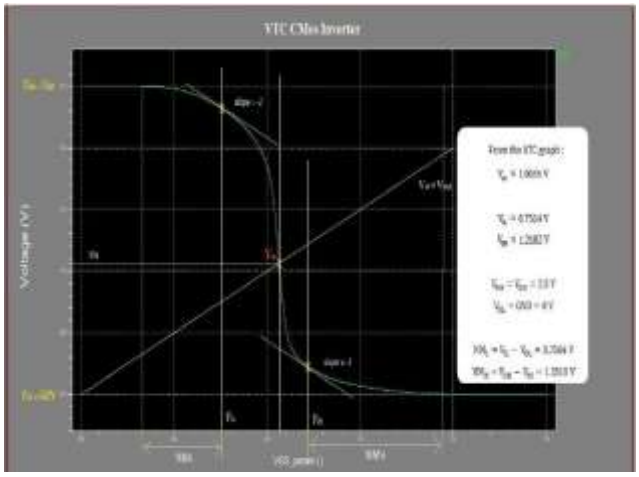

Fig2 VTC analysis curve of an inverter

VIII. CONCLUSION

The main intention of all paper is to provide good power consumption by using many techniques. In static random access memory many related issues like power minimization, reduce switching , size scaled down can be solved by using different Technologies like Advanced Stacked sleep technique, forward bias technique and pre-charge technique, quiet bit line technology and many more technologies has been proposed.

T-Spice simulations used to validate the proposed method show significant power reduction during test (~50%). SRAM cell with dual VDD technique show a reduction of 96% in total leakage power. A novel SRAM 6T cell operates by charging/discharging of a single bit-line (BL) during read and write operation, resulting in reduction of dynamic power consumption to only 40% to 60% (best case / worst case) of that of a conventional 6T SRAM cell.

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