DESIGN OF CURRENT MODE R-2R LADDER DIGITAL TO ANALOG CONVERTER USING SWITCHABLE MOS DEVICES

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ABSTRACT

This paper present a design of Current mode MOS only R-2R ladder Digital to Analog converter using an innovative technique for dividing currents accurately. The resistances in conventional R-2R ladder Digital to Analog Converter are replaced by NMOS as switch which has lower power & area. The design of R-2R ladder is supported by current mode architecture which results efficient reduction in power dissipation. The design is supported by implementation of 4 bit R-2R ladder network using NMOS transistors only. Four bit D to A converters use an LSB current of 10uA and implemented using 180nm CMOS process.

Keywords: Digital To Analog Converters, NMOS, R-2R Ladder.

I. INTRODUCTION

The 4 bit digital to analog converter is implemented by current mode R-2R ladder architecture. This Design is elaborated by the concept of division of current or voltages very accurately & linearly in various signals processing application like A/D, D/A conversion. A common technique is to use resistors or capacitors for the linear & accurate division of current or voltage while using NMOS as switches. In this paper, 4 bit current mode R-2R ladder D/A is proposed based on the NMOS as switch for linear current division technique.When we design 8 bit D/A converter directly the requirement of total reference current will be 256 times the 1LSB current. Hence this current is too large for MOS device to handle. Instead of handling large current we have design 4 bit R-2R ladder Digital to Analog converter and each stages are handling total reference current of160uA. Section II presents the basic MOS current division principal. Section III reviews the design of linear current mode 4-bit R-2R ladder DACs. In Section IV discuss the power dissipation analysis. Section V gives results of Current mode R-2R ladder DAC. Section VI gives the conclusion of the design.[1]

II. THE MOS CURRENT DIVISION PRINCIPAL

The basic principal of current division technique is shown in fig 2. Both NMOS transistor have the same gate voltage Vg. The two terminal voltages Vx & Vy can be select such that the transistors are in the on state. A

current I_{in} flowing into or out of the circuit will be divided into two parts, in which I_1 flow into Vx, & I_2 flow to Vy. The current division principal state that the fraction of this input current flowing to one side is:

1) Constant & independent of I_{in}
2) Independent of the values of Vx &Vy.
3) Independent of whether one or both device operates in linear or in saturation region.

That is why the basic current division technique independent of process variations and thus well suited for large scale integration.Note that Vx and Vy may be any value applied, there may be a dc current flowing through the transistor. Also assume that Vx and Vy are ideal voltage source, i...e, having zero output impedance. Current division ratio is independent of voltages Vx, Vy, Vg and I_{in}, the operation of two MOS devices is only depends on the aspect ratio of the devices [1].

$$\frac{\Delta I_1}{\Delta I_2} = \frac{\frac{W_1}{L_1}}{\frac{W_2}{L_2}} \quad (1)$$

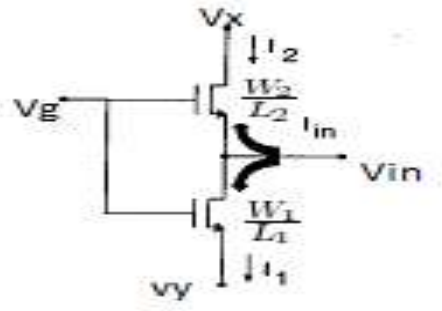

Fig. 1: The principle of current division

All transistors in R-2R ladder D/A converter are biased in linear region and having large aspect ratio. Because the current division mechanism is based on the symmetry of a MOS device and it is valid for both NMOS & PMOS [2].

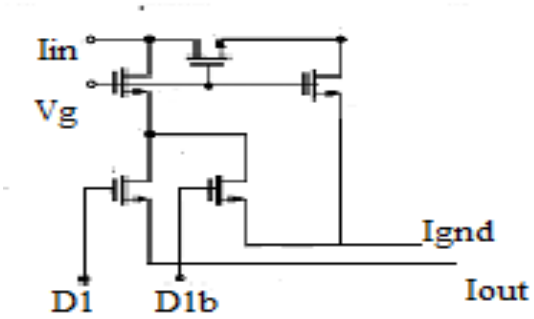

Fig.2: The unit cell of R-2R ladder using NMOS

III. DESIGN OF R-2R LADDER D/A CONVERTER

The design of current mode 4 bit R-2R ladder D/A converter is shown in fig 3. The resistances in R-2R ladder D/A converter are replaced by NMOS as switch, and are biased in strong inversion region to reduce the power dissipation. All transistors are having same gate voltage and aspect ratio (W/L) to avoid the transistor mismatch. The conventional resistive R-2R ladder is shown in Fig 4. The 4 bit R-2R ladder D/A converter consist of 17 NMOS transistors as shown in Fig. 4. All NMOS transistors have same aspect ratio given in table I.

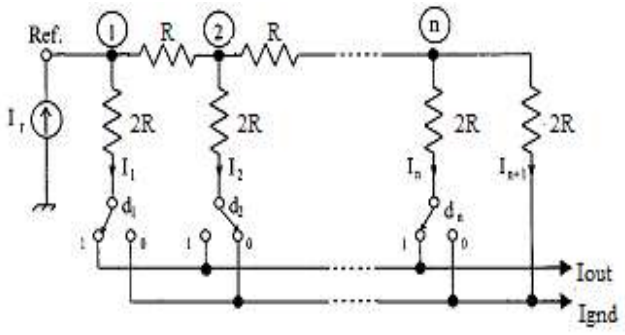

Fig.3: n-bit Resistive R-2R ladder

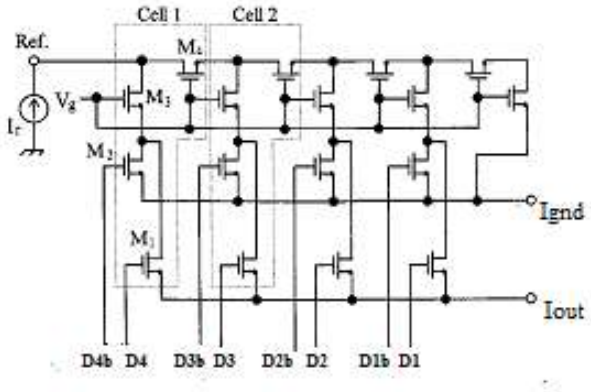

Fig.4: The 4 bit R-2R ladder D/A Converter.

In this design, 1LSB current is chosen to be 10uA. Hence for 4 bit the total reference current will be 2^4 times the 1LSB current i...e, $I_{ref} = I_{in}$= 160uA. The fig. 4. shows the schematic of 4 bit LSB R-2R ladder D/A converter. All NMOS transistors in the design have same gate voltage and aspect ratio given in Table I.

Table I

Process Parameters	Specifications
CMOS Process	180nm
V_T	0.37 V
un * Cox	246.90uA/V^2
W	60um
L	1um

Assume that four NMOS transistors as shown in fig. 4 are matched and operate in linear region .The drain current of NMOStransistors M1 and M2 operating in the linear region is given by [4]

$$I1 = \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)_1 (V_g - V_s - V_T)(V(1) - V_s) \quad (2)$$

$$I2 = \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)_2 (V_g - V(2) - V_T)(V(1) - V(2)) \quad (3)$$

Where I1 and I2 are the current through the transistors M1 and M2 respectively, μ_n is the mobility of the electron, Cox, (W/L) and V_T are the oxide capacitance aspect ratio and threshold voltage of the transistors respectively [3,4].

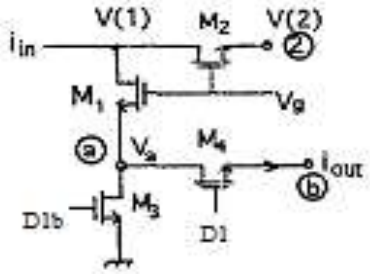

Fig. 5: The unit cell of 4 bit R-2R ladder D to A converter.

The aspect ratio of the transistor should be large in order to achieve small on channel resistance of MOS Device which reduces the power dissipation & harmonic distortion [4].

The output current equation is given by

$$Iout = (D4\ 2^{-1} + D3\ 2^{-2} + D2\ 2^{-3} + D1\ 2^{-4}) \times Iref(4)$$

WhereIout = output current

Iref (total reference current) =160uA.

D4, D3, D2 & D1 are digital inputs.

D4 is MSB bit and D1 is LSB bit.

Table II. Shows the relationship between digital inputs and analog output.

Table II

Digital Input				Analog output
D4	D3	D2	D1	Iout (µA)
0	0	0	0	0
0	0	0	1	10
0	0	1	0	20
0	0	1	1	30
0	1	0	0	40
0	1	0	1	50
0	1	1	0	60
0	1	1	1	70
1	0	0	0	80
1	0	0	1	90
1	0	1	0	100
1	0	1	1	110
1	1	0	0	120
1	1	0	1	130
1	1	1	0	140
1	1	1	1	150

From the table II we conclude that Output current is increasing in the step of 10µA and is always less than 1 LSB current. The total output current swing will be upto 150µA. Table III shows the simulation conditions.

Table III

Parameter	Conditions
Reference Current	Iref = 160uA
Transistor dimensions	W = 60um, L = 1um
Gate bias Voltage	Vg = 0.8 V
Logic levels	0.8 V when Di = 1 and 0 V when Di = 0

IV. RESULTS

Fig. 6 & Fig. 7 show the output current waveform of current mode 4 bit R-2R ladder digital to analog converter.This shows that the Resistances in conventional R-2R Ladder can be replaced by NMOS as switch which can be used in digital to analog converter.It improves linearity, INL & DNL values for this digital to analog converter.

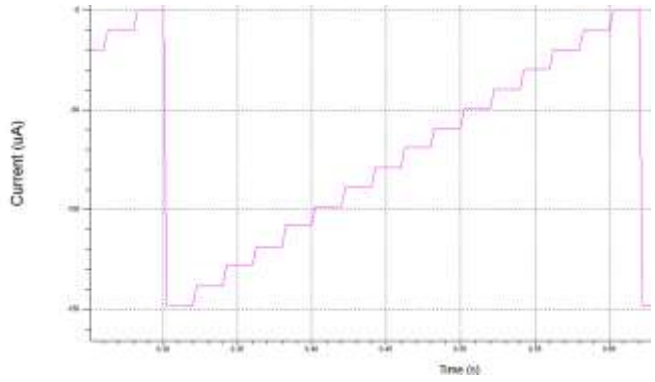

Fig.6: Output waveform of current 4 bit R-2R ladder D/A converter.

Fig.7: Output waveforms of voltage 4 bit R-2R ladder D/A converter.

V. CONCLUSION

The Design of 4 bit current mode R-2R Ladder Digital to Analog converter using switchable MOS Devices has been proposed and implemented successfully. This Design is independent of threshold voltage, terminal voltages and process parameter but it depends on W/L ratio of all transistors in the current mode R-2R ladder Digital to Analog converter. But it depends on W/L ratio of all transistors in the current mode R-2R ladder D/A converter. Power dissipation reduces significantly in this current mode digital to analog converter.

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