FPGA IMPLEMENTATION OF LOW POWER RCHITECTURE FOR ADAPTIVE NOISE CANCELLATION

K.Vaishnavi[1], Dr. K.N.Vijeya Kumar[2]

[1]Department of Electrical & Electronics Engg., Dr.MCET, Pollachi .,Tamilnadu (India)

[2]Associate professor., Department of Electrical & Electronics Engg., Dr.MCET, Pollachi .,Tamilnadu (India)

ABSTRACT

This paper presents the VLSI implementationof Adaptive noise cancellation based on LMS algorithm. The main goal of this paper is to reducing the noise signal and also to verify the functionality and performance of the noise cancellation using audio input. At the beginning the adaptive parameters are obtained by simulating Noise cancellation on MATLAB. Simulink model of adaptive noise canceller was developed and the noise is suppressed to a much larger extent in recovering the original signal. The given elements of input and output signals, desired signal, step size factor and coefficient so adaptive filter was processed by FPGA .After that, the functionality of the FPGA based system structure for Adaptive noise cancellation on Least Mean Square algorithm was simulated, implemented and synthesized on Spartan-6 FPGA XC6SCX45T-2CSG324 board. Area and timing reports are given for particular target device. The power dissipation of 0.084W is obtained and the proposed system for different clock frequencies is estimated using Xilinx ISE 12.1 tool.

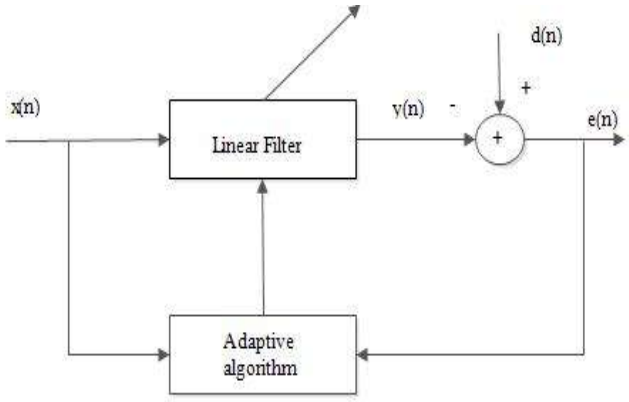
Key Words– LMS Algorithm , Adaptive Filter, Error Estimation, MATLAB/SIMULINK, Spartan - 6 FPGA XC6SCX45T-2CSG324 XILINX ISE 12.1.

I.INTRODUCTION

Speech is a very basic way for humans to convey information. It has a bandwidth of only 4 kHz; it can convey information with the emotion of a human voice. Certain properties of the speech signal are, it is a one dimensional signal, with time as its independent variable, it is random source in nature, and also it is non-stationary, and the frequency spectrum is not constant in time. Although human beings have an audible frequency range of 20 Hz to20 kHz, the human speech has significant frequency components only up to 4 kHz .The most common. problem in speech processing is the effect ofinterference noise in the signals[8]. This noise masks the speech signal, reduces its intelligibility and also in noisy environment speech communication is greatly affected by the presence of background acoustic noise. The presence of background noise in speech significantly reduces the intelligibility of speech. Noise reduction algorithms are used to suppress such background noise and improve the perceptual quality and intelligibility of speech. Removing various types of noise is difficult due to the random nature of the noise and the inherent complexities of the speech. The performance of noise cancellation technique using adaptive filters depend on the quality and intelligibility of the Processed speech signal. The improvement in the speech signal to noise ratio is the target of this technique.[11]

II.ADAPTIVE FILTER

Adaptive filter automatically adjusts the parameters of the system to achieve optimal performance according to some criteria. Adaptive filters are having wide range of applications such as noise cancellation, System identification, channel equalization and beam forming etc. The block diagram of adaptive filter is shown in Fig.1.Adaptive filters are generally designed as finite impulse response (FIR) filters due to the fact that these filters can provide a linear phase response and always stable.



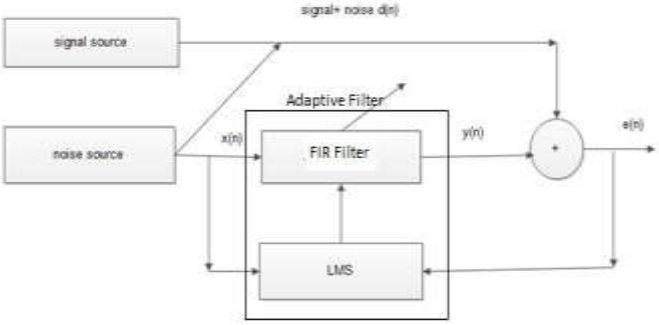


Fig.1: Block diagram of Adaptive filter **Fig.2 :Block diagram of Adaptive noise cancellation**

Least Mean Square algorithm (LMS) is used to implement adaptive noise canceller because of its simplicity and low complexity. Performance of adaptive filters using LMS algorithm is better in relation with the number of iterations required for convergence when compared with other algorithms. The design tools should be chosen carefully as the signal processing applications enforce substantial limits on area, power dissipation, speed and cost. Digital signal processors (DSPs), Field programmable gate arrays (FPGAs) and application specific integrated circuits are the most widely used tools for the design of such application. The DSP used for every complex math-intensive tasks but can't process great sampling rate applications due to its architecture. ASIC faces lack of flexibility and need extensive design cycle. The limitations of DSP and ASIC are overcome by single FPGA [4]. Therefore FPGA has become the best choice for the signal processing system designs due to their greater flexibility and greater bandwidth, resulting from their parallel architecture[5].

This paper is structured as follows : Section III gives brief overview of LMS algorithm and weaknesses of current techniques .Section IV presents the proposed system of noise cancellation. Section V shows the hardware implementation and software simulation results and section VI is conclusion of the paper. This paper investigates the applicability of FPGA system for adaptive noise cancellation[6] ineffective and in expensive way.

III.LMS ALGORITHM

The least mean squares (LMS) algorithms adjust the filter coefficients to minimize the cost function Compared to recursive least squares (RLS) algorithms, the LMS algorithms do not involve any matrix operations. Therefore, the LMS algorithms have fewer computational resources and memory than the RLS algorithms. The

implementation of the LMS algorithm is less complicated than the RLS algorithm.[5] However, the Eigen value spread of the input correlation matrix, or the correlation matrix of the input signal, might affect the convergence speed of the resulting adaptive filter. Least mean squares (LMS) algorithm are a class of adaptive filter used to mimic a desired filter by finding the filter coefficients that relate to producing the least mean squares of the error signal (difference between the desired and the actual signal).The least mean squares (LMS) algorithms adjust the filter coefficients to minimize the cost function. And it require fewer computational resources and memory. The implementation of the LMS algorithms also is lesscomplicated. The output of the filter y (n) is given by Equation (1),

$$y(n) = w^T(n)x(n) \quad (1)$$

Where w (n) is weight vector and the error signal is given by Equation (2),

$$e(n)=d(n)-y(n) \quad (2)$$

Substituting (1) in (2) yields

$$e(n)=d(n)-w^T(n)x(n) \quad (3)$$

According to the mean square error criterion Optimum filter parameters Wopt should make £=E{e^2(n)}, as minimum.

The mean square error can be expressed as in Equation (4),

$$£=E\{d^2(n)\}-2w^Trxd+w^TRxxw \quad (4)$$

Where rxd =E{x(n)d(n)}, is cross-correlation vector and Rxx = E{x(n)X^T (n)}, is autocorrelation matrix. It can be seen that the mean square error is a quadratic function of Wopt, and the matrix Rxx is positive definite or positive semi definite, so it must have a min value. Due to this gradient of W is zero, so the minimum when wopt meet Δ£=0 and when Rxx get a unique solution wopt=Rxxrxd, is considered.In LMS algorithm the gradient of the instantaneous squared error can be used instead of the gradient of the mean square error. To update the weights for each iteration of theAdaptive filter a step size parameter μ is introduced to control speed of convergence of the algorithm.

$$w(n+1) = w(n) + 2\mu e(n)x(n) \quad (5)$$

The step size parameter affects the stability, convergence speed and steady state error, so to reduce steady state error Small step size is used but it decreases the speed of the convergence of the algorithm. For better speed of convergence the step size value is increased but this affects the filter stability.

IV. ADAPTIVE NOISE CANCELLATION

Adaptive noise cancellation algorithms utilize two signal. One signal is used to measure the speech + noise signal while the other is used to measure the noise signal alone. The technique adaptively adjusts a set of filter coefficients so as to remove the noise from the noisy signal. This technique, however it requires that the noise component in the corrupted signal and the noise in the reference channel have high coherence. With large separations the coherence of the noise is limited and this limits the effectiveness of this technique.

Figure.2 shows the adaptive noise cancellation setup. In this application, the corrupted signal passes through a filter that tends to suppress the noise while leaving the signal unchanged. This process is an adaptive

process, which means it cannot require a priori knowledge of signal or noise characteristics.[12] .An adaptive filter automatically adjusts it shown impulse response through an LMS algorithm. The key objective of this paper is to provide an idea for FPGA Implementation of LMS algorithm for Adaptive Noise Canceller. Xilinx Spartan6 FPGA is used for synthesis [11].The advantage of the process is its adaptivity and real time application.

V. RESULTS AND DISCUSSION

5.1 MATLAB simulation

The design implement the FIR filter with 5 taps. The coefficients for the filter are extracted using Remez command in MATLAB. The speech signal having the frequency of 16 Hz is used as the input. A bird's eye view of the speech signal is used as the input for the system. The speech signal is desired using samples and the sample values are used as the inputs for the system.Gaussian noise generator is used as the error signal. So in the LMS filter block input signal, desired signal, adaptive, step size and reset input ports. And output , error are used as the output ports. In noise cancellation, the Gaussian noise is given to the input signal and Gaussian noise + speech signal is given to the desired signal. Then output signal from LMS filter is given to the input of the Adapt port ,step size is maintained at 0.002.Then the output is connected to the audio device. Figure.3 shows The Simulink implementation of the noise cancellation system.

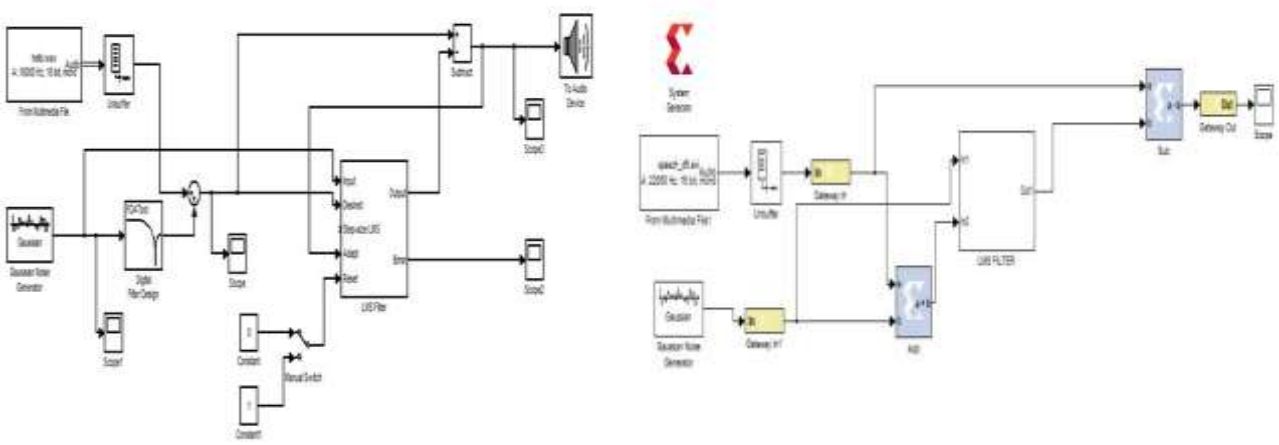


Fig.3: Simulink model of adaptive noise cancellationFig.8 :Xilinx model of simulink implemention of ANC

5.2 MATLAB simulation results

Environmental noise polluted sinusoidal signal is extracted. Noise signal is modelled as Gaussian noise. The two signals are added and are used as the inputs for of LMS adaptive filter. The other input to the noise cancellationsystem is Gaussian noise signal. The qualities of outputs are examined to interpret the characteristics of the noise cancellation system. Evaluation of the proposed noise cancellation system is done through simulation outputs for the various steps sizes. If the step size parameter is kept high the response is fast but is less accurate and vice versa.The difference of desired Signal and Input Signal is the error Signal which is obtained from error Signal output port of LMS block. The Signal from this port is the Filtered Signal from

which Noise has been adaptively removed out.[7]

The error signal value decreases as the iteration proceeds and emulating the desired signal more effectively cancelling the noise. MATLAB simulations are carried out with different steps size to optimize the step size for better convergence of the algorithm. Adaptive parameters are obtained through MATLAB simulations are used as the inputs for the hardware to be implemented on FPGA. The Figure.4 and 5 shows the input Gaussian noise signal and desired signal respectively.Figure.6, and Figure.7 shows the adaptive noise canceller Simulink Model scope output. Figure.4 represents noisy signal entering into the system. Figure.5shows the noisy and speech signal entering into the system. Figure .6 shows the signal obtained after Adaptive filtering. By varying the step size parameter of LMS for noise cancellation is observed. Higher the step size, fast the convergence rate.

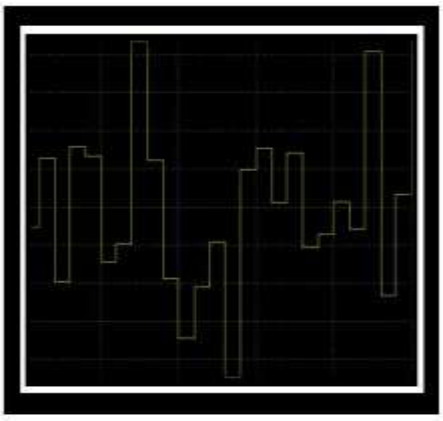


Fig.4: input Gaussian signal

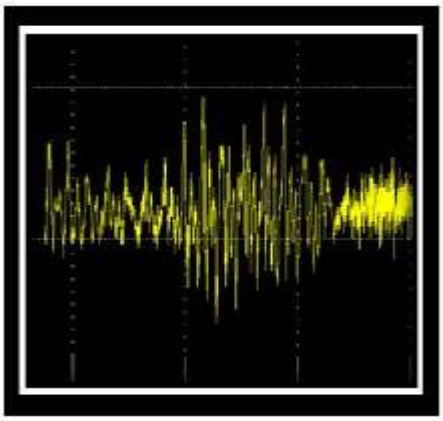


Fig.5: desired signal

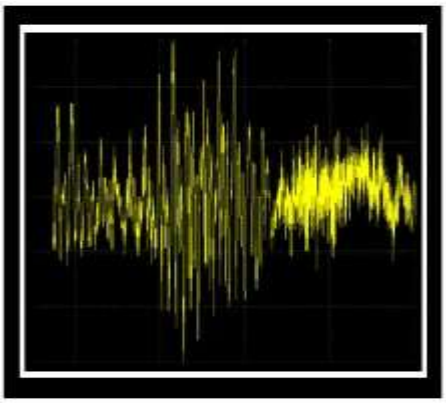


Fig.6: original speech signal

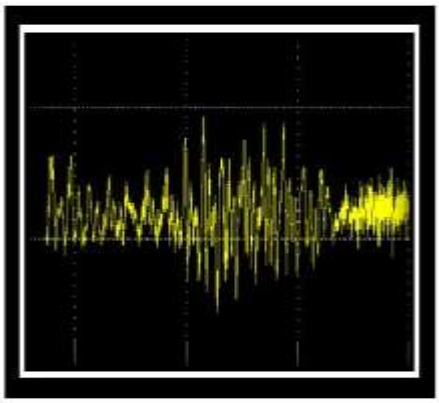


Fig.7: Error signal

5.3 FPGA implementation using Xilinx

The Simulink implementation of the noise cancellation system is shown in Figure.8. It consists of 3 blocks: Input signal, desired signal and Adaptive filter. Here x(n) is the analog input signal which is applied to the one of the input of adaptive filter. Which convert analog to digital form ,the output of the digital filter block is d(n).[3]

The Xilinx 12.1 development environment was used for implementation of MATLAB design. The design has been transferred to VHDL code and it's the hardware simulation done with the Xilinx ISE simulator and also

implemented on Spartan-6 FPGA XC6slx45t-2csg324 board.Apply x(n) the input random signal with 1024 samples and d(n) to the Adaptive FIR filter . The adaptive filter starts compare d(n) with x(n) and produces the output e(n). The Adaptive FIR Filter updates the coefficients using LMS algorithm based on the error signal generated using input speech signal and estimated output of adaptive filter.

5.4 .Xilinx results

The input signal of Gaussian noise is sampled and that is fed to the one of the input of Xilinx Model[3]. The desired signal of Gaussian noise and speech signal is also sampled and that is given to the another input of Xilinx model. In this Xilinx model have to discuss about the minimum period required for system, combinational path delay, maximum frequency required for the system and power dissipation of the system.The test bench is developed in order to test the modelled design. This developed test bench will automatically force the inputs, which are taken from the reference, and will make the operations of algorithm to perform. Timing reports include total time delay for output to appear after giving input.

At speed grade of -12, design operates at maximum frequency of 135.66MHz.Theminimum period require is 7.376ns and combinational delay is 3.723ns.The power dissipation of the proposed architecture for different clock frequencies is estimated by Xilinx Power tool 0.084watts. The proposed design implemented on Spartan 6 based FPGA can work at maximum operating frequency. The total power consumption of the proposed design based on XC6SCX45T-2CSG324FPGA device has been calculated.The simulation results showed in below Figure.9.The values of x (n) are stored in a delay register and registers are required for each weight coefficient. Each unit contains a slice of the shift registers, an adder and a multiplier. It also consist an output register, but this is optional. Table.1 shows the Xilinx device utilization summary.TABLE.II represents the performs comparison of Vakulabharanam Ramakrishna & Tipparti Anil Kumar(2013) where in the base design and previous works viz., Sujith Chatrad & Asha (2013), Jebin Roy & Ramya (2014) designs. In previous work ,the power dissipation of the noise cancellation system is high and combinational path delay also high.

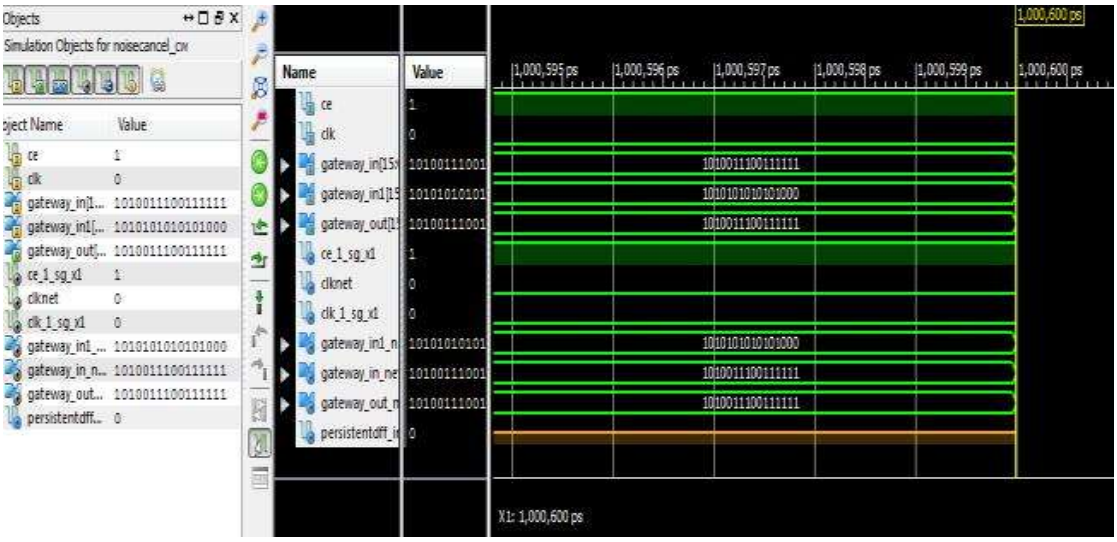


Fig.9: Output waveform of proposed ANC

The proposed method reduces the Area ,power dissipation and Combinational path delay.The design operates at maximum frequency of 135.66MHz.The minimum period require is 7.376ns and combinational delay is

3.723ns.The power dissipation of the proposed architecture for different clock frequencies is estimated by Xilinx Power tool 0.084watts. The proposed design implemented on Spartan 6 based FPGA can work at maximum operating frequency. The total power consumption of the proposed design based on XC6SCX45T-2CSG324 FPGA device has been calculated.

TABLE.I Device utilization summary of ANCTABLE.II represents the comparison of previous work and proposed work of the noise cancellation system.

noisecancel_cw Project Status (11/28/2014 - 15:13:02)			
Project File:	noisecancel_cw.xise	Parser Errors:	No Errors
Module Name:	noisecancel_cw	Implementation State:	Placed and Routed
Target Device:	xc6slx45t-2csg324	• Errors:	No Errors
Product Version:	ISE 12.1	• Warnings:	208 Warnings (45 new)
Design Goal:	Balanced	• Routing Results:	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	• Timing Constraints:	1 Failing Constraint
Environment:	System Settings	• Final Timing Score:	19660 (Timing Report)

Device Utilization Summary				
Slice Logic Utilization	Used	Available	Utilization	Note(s)
Number of Slice Registers	204	54,576	1%	
Number used as Flip Flops	176			
Number used as Latches	0			
Number used as Latch-thrus	28			
Number used as AND/OR logics	0			
Number of Slice LUTs	154	27,288	1%	
Number used as logic	146	27,288	1%	
Number using O6 output only	116			
Number using O5 output only	0			
Number using O5 and O6	30			

Design	Power dissipation (Watts)	Delay(ns)	Max. Operating frequency (MHz)
Sujith Chatrad & Asha (2013)	0.156	3.738	137
Jebin Roy & Ramya (2014)	0.1789	3.76	105
Base paper - Vakulabharanam Ramakrishna & Tipparti Anil Kumar(2013)	0.084	3.723	135.66

VI.CONCLUSION

The method of Adaptive noise cancellation System provide a signal free from noise. The adaptation of filter coefficients is effected using LMS algorithm technique. The LMS algorithm is suggested to reduce the number of coefficients for low computational complexity. Through implementation and survey it has been found out that using pipelined architecture as computational unit makes implementation of adaptive filters easier. Numbers of registers and delays were adjusted the coefficient value to achieve speed of operation, while minimizing approximation error. The implementation results of adaptive noise cancellation system in Spartan 6 FPGA board revealed better area and power reduction compared to power approaches with the power consumption of 0.084 watts. In addition with the proposed approach there is a high possibility for pipelining to achieve higher throughput facilitating real time implementations.

REFERENCES

[1]. Arunkumar,.Parthiban, .AravindKumar,(2013) "Implementation of Least Mean SquareAlgorithm for sinusoidal and audio denoisingusing FPGA", International Journal of Advanced Research in Electrical, Vol. 2, Issue 12.

[2]. AshuSharma&YogeshJuneja,(2014) "Acoustic Echo Cancellation fromthe Signal Using LMS Algoritl International Journal of Research in Advent Technology,Vol.2,No.6.

[3]. GyanendraSingh ,Kiransavita, ShivkumarYadav,(2013) "Designof AdaptiveNoise Canceller using LMSAlgorithm",IJATER Vol.3,Issue 3.

[4]. IanKuon,(2007) "Measuring the gap between FPGAs and ASICs",IEEE Transaction on Computer – A ntegrated Circuits and Systems,Vol. 26, No. 2.

[5]. JyotsnaYadav,Mukesh Kumar, RohiniSaxena, Jaiswal,(2 ıceAnalysisofLMSAdaptiveFIRFilter and RLS AdaptiveFIIRFilter for Noise Cancellation", SIPIJ V

[6]. JebinRoy.&Ramya, (2014)"Low Power and Low AreaAdaptive FIR Filter based Algorithm"International Journal ofScientific andResearchPublications,Volume 4, Issue 3.

[7]. Oravec ., Kadlec , Cocherová .(1999) " Simulation of RLS and LMS algorithms forAdaptive noise cancellation in MATLAB",International Journal of Adaptive control and signalprocessing, vol. 13.

[8]. Rafael Ramos, (2007) "FPGA - based Implementation of an Adaptive Canceller for50/60-Hz Interference inElectrocardiography", IEEE Transactions on Instrumentationand Measurement, Vol

[9]. RupaliMane&Kolte,(2014)"Implementation of Adaptive FilteringAlgorithmforSpeechSignal FPGA",IJIREEICEVol. 2, Issue 3.

[10]. Sathesh&. Muniraj, (2012) " Separation of Heart Sounds fromLungSoundsusing LMS Adaptive EqualizerImplementation in Cadence Tools",IJMSE Vol. 2, No.1.

[11]. Shashikalaprakash, Renjithkumar ,Subramani,(2013) "An FPGA Implementation of theLMS Adaptiv FilterFor

[12]. Active Vibration Control, IJRET volume: 02 Issue: 10
VakulabharanamRamakrishna&TippartiAnil Kumar, (2013)"Low Power VLSIImplementation AdaptiveNoise
Canceller based onLeastMean Square Algorithm",IEEE Transactions on Circuits and Systems - Ii: V No.60.