EMBEDDED Z- SOURCE INVERTER H –BRIDGE

ArchanaMishra[1], K.M.Tripath[2]

[1] *Department of Electrical and Electronics, K.I.E.T, Ghaziabad, (India)*

[2]*Associate Professor & Head of Electrical and Electronics Department,*

I.T.M GIDA, Gorakhpur (India)

ABSTRACT

The present work deals with an Embedded Z-source inverter in which various voltage and current circuities is represented as a single unit and inverter follows buck –boost energy conversion technique. The shoot through state by which two semiconductor switches of the same phase leg can be turned ON simultaneously is a unique feature of EZ source inverter. This feature gives an advantage of improved reliability and reduced output distortion asno dead time is needed .These inverter remove the drawback of traditional voltage source and current source inverters. The loads demanding a high voltage gain to match the input source voltage differences such as power conditioning unit for renewable energy sources fuel, solar cell and motor drivesetc. require EZ source inverters .These EZ inverters are safe to use and complexity is also greatly reduced.The designing of EZ-source inverters can be made by using only passive elements excluding additional active semiconductor. These latter features are attained without using any additional passive filter which surely is a favorable advantage since an added filter will raise the system cost and, at certain time can complicate the dynamic tuning and resonant consideration of the inverters. Removal of additional passive filter cheap and low harmonic distortion produce a smaller current or voltage maintained across the dc input source. To demonstrate these features analysis, simulation, and experimental results were carried out.

Keyword: Embedded Z-Source Inverters, Motor Drives, Buck-Boost, Z-Source Inverters.

I. INTRODUCTION

Power Converters are used for electrical power processing. To overcome the problems of the traditional V-source and I-source converters, an impedance-source (or impedance-fed) power converter (abbreviated as Z-source converter) and its control method for implementing dc-to-ac, ac-to-dc, ac-to-ac, and dc-to-dc power conversion. It employs a unique impedance network (or circuit) to couple the converter main circuit to the power source, load, or another converter, for providing unique features that cannot be observed in the traditional V- and I-source converters where a capacitor and inductor are used, respectively. In Z-source inverter there is a two-port network that consists of a split-inductor and capacitors and connected in X shape is employed to provide an impedance source (Z-source) coupling the converter (or inverter) to the dc source, load, or another converter. The dc source/or load can be either a voltage or a current source/or load. Therefore, the dc source can be a battery, diode-rectifier,thyristorconverter, fuel cell, an inductor, a capacitor, or a combination of those. Switches used in the converter can be a combination of switching devices and diodes. The Z-source converter (ZSC) topology[1] in power conversion, which has unique features that can overcome the limitations of VSI and

CSI, fig (1) shows the ZSC implemented as a 3-phase DC/AC converter (inverter). Although DC/AC conversion is the most common application of the Z-source topology, it can also be applied to AC/DC and AC/AC power conversions [3]. The X shape impedance is the Z-source network which is composed of two split inductors and two capacitors to provide a coupling between the DC source and the inverter bridge. The Z-source inverter (ZSI) has the unique buck-boost capability which ideally gives an output voltage range from zero to infinity regardless of the input voltage. This is achieved by using a switching state that is not permitted in the VSI which is called the -shoot-through state. This is the state when both upper and lower switches of a phase leg are turned on. In a conventional VSI switching pattern, there are eight permissible switching states. Six of those switching states are called the - active states where the load sees the input voltage and the remaining two states are called the - zero states where either the entire upper or all the lower. The idea behind this is that when we look from the Z-source network point of view, in the shoot-through, the Z-source network is shorted and in the active state, the Z-source network sees the load. In this circuit fig (1) when the parallel switch S2 is on, the Z-source impedance network is shorted and the load sees zero voltage. Similarly, when S2 is off the Z-source network sees the load and active state occurs. It can be observed that the dc-link voltage has a pulsating nature. For simplification purposes, Z-source network parameters are selected as; L_1=L_2 and C_1=C_2which makes the Z-source network symmetrical [2],-[5]. Accordingly, the capacitor and inductor voltages of the Z-source network become,

$V_{C1}= V_{C2}= V_C$ (1)

$V_{L1}= V_{L2}= V_L$

Given that the converter is in the shoot-through state for an interval of during a switching cycle, from the equivalent circuit in fig (1) we have,

$V_L=V_C$ and $V_{dc}=0$ (2)

Similarly, if the converter is in the active state for an interval of T_1,during the switching cycle T, from the equivalent circuit in fig(1) wehave [6],

$V_L= V_g- V_C$ and

$$V_{dc}= V_c-V_L = 2V_C- V_g \quad (3)$$

Where is the DC source voltage and. T_0=T_1+T_2

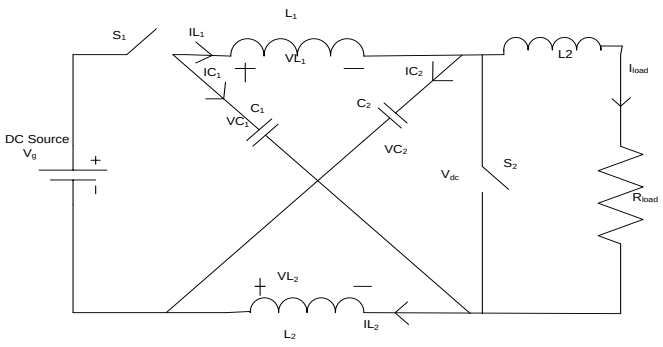

Fig .1: Simplified ZSC

The average value of the voltage across an inductor for a switching period (T) is zero in steady state, so from Eq. (2) and Eq. (3) we have [3],

$$\frac{1\int_0^T V_L((t)}{T}=\frac{T_0V_C+T_1(V_g-V_c)}{T}= 0 \quad (4)$$

Or

$$\frac{V_c}{V_g}=T_1/(T_1-T_0) \quad =\frac{1-D}{1-2D}\frac{V_c}{V_g}=\frac{T_1}{T_0} \qquad (5)$$

Where $D=T_0/T$ is the shoot-through duty cycle, V_c is the steady state (DC) value of the capacitor voltage and Vg is the steady state value of the input voltage. The peak value (V_{DCR}) of the pulsating dc-link voltage (V_{dc}) is expressed in Eq. (3) and it can be rewritten in steady state as [3],

$V_{den}=2V_C-Vg=\frac{T_1}{T_1-T_0}Vg=\frac{1}{1-2D}Vg=BV_g$ (6)Where *B* is known as the boosting factor based on, and is the steady state value of the peak dc-link voltage. Eq. (6) gives the voltage conversion ratio of the ZSC.Since D is between zero and 0.5,can take any value between one and

$$V_{ac}=M\frac{V_{dcn}}{2} \quad (7)$$

Where, M is the modulation index of the inverter. Using Eq. (6), Eq. (7) can be rewritten as

$$V_{ac}=MB\frac{V_g}{2} \quad (8)$$

Eq.(8) has an additional multiplication factor of compared to the VSI voltage conversion ratio which gives the boosting capability to the Z-source inverter. Consider the H-bridge Z-source inverter in fig(2),the active and null states in which the two switches of a phase-leg are switched complementary, are common to both conventional VSI and the H-bridge Z-source inverter. However, the remaining three shoot-through states in which one phase-leg (H1 and H2) or two phase-legs (H3) are short-circuited, are unique to the H-bridge Z-source inverter [4].When in a shoot-through state, the Z-source inductor currents are boosted but the inverter output voltage is kept at 0V, similar to that of a null state where the AC load is short-circuited. Therefore, for a fixed frequency, inserting of shoot-through states within the null intervals with the active state intervals maintained constant will not alter the normalized volt–sec average per switching cycle. This feature allows all existing volt–sec PWM methods to be used for controlling a Z-source inverter with only minor modifications added to insert the shoot-through states [4].

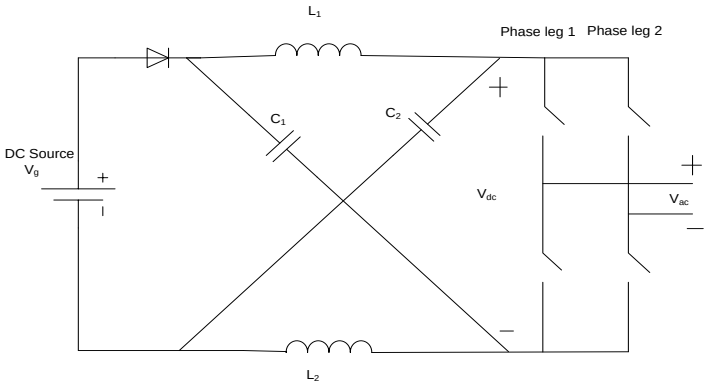

Fig. 2: H bridge (single phase) Z source inverter

The formulation of modulating reference signals are needed for carrier-based Z-source inverter modulation. For a conventional VSI, the reference signals used are $V_a=M\cos(\omega t)$ for modulating phase-leg {*SI*,*S4*}, and $-V_a$for phase-leg {*S3*, *S6*}. In general, the first state transition during the falling carrier edge occurs when the maximum of the two signals $V_{max}=\max(V_a, -V_a)$crosses the falling slope of the carrier at time tH1. In order to

insert a shoot-through state adjacent to this transition from t_{H1} - $0.5t_o$to t_{H1}, the upper (odd-numbered) and lower (even-numbered) switches of the relevant phase-leg should therefore be modulated using

$$V_{max(sx)}=V_{max(sy)}+\frac{T_0}{T}(9)$$

$$V_{max(sy)}=V_{max}(10)$$

Where V_{max} causes the upper switch to turn ON at t_{H1} - $0.5t_o$ and $V_{max(xy)}$causes the lower switch to turn OFF at $t_{H1.}$ Obviously, these switching actions insert the desired shoot-through state H1.Following through similar analysis, the second shoot-through state H2 can be inserted from at $t_{H2}$to at t_{H1} + $0.5t_o$by using the following modified reference signals for controlling the other two switches

$$V_{min(sy)}=V_{min}-\frac{T0}{T}(11)$$

$$V_{min(sy)}=V_{min}(12)$$

Where V_{min}=min ($V_{a,}$-V_a) represents the minimum of $V_{a,}$ and -$V_{a,.}$Without modification, the same derived equations (12) and (14) can also be used for ensuring the correct insertion of shoot-through states during the rising carrier edge.The voltage stress under simple boosting modulation method can be calculated by,

$$V_S=BV_g=(2G-1)\,Vg \quad (13)$$

The voltage stress for the maximum boosting method is derived

$$V_S=B_g=(\frac{3\sqrt{3}G}{\pi}-1)\,Vg(14)$$

II. MODELLING OF EMBEDDED ZSE

The voltage-type EZ-source inverter shown in fig(3) has its dc sources embedded within the X- shaped *LC* impedance network with its inductive elements *L*1 and *L*2 now, respectively, used for filtering the currents drawn from the two dc sources without using any external *LC* filter[13]. The impedance network used buck or boost the input voltage depends upon the boosting factor .This network also act as a second order filter .This network should require less inductance and smaller in size. Similarly capacitors required less capacitance and smaller in size. The output voltage from impedance network is fed to the three phase inverter main circuit. The inverter main circuit consists of six switches. Gating signals are generated from the driving circuit. Depends upon the Gating signal inverter operates and the output of inverter is fed to the R-L load. When the two inductors (L_1 and L_2) are small and approach zero, the Impedance source network reduces to two capacitors (C_1 andC_2) in parallel and becomes traditional voltage source. Similarly, when the two capacitors (C_1 and C_2) are small and approach zero, the Impedance Source Network reduces to two inductors (L_1 and L_2) in series and becomes a traditional current source. Therefore considering additional filtering and energy storage by the capacitors, the impedance source network should require less inductance and smaller size compared with the traditional current source inverters.

III. MATHEMATICAL ANALYSIS OF EMBEDDED IMPEDANCE NETWORK

The switches that are from the same phase-leg can be turned on simultaneously to introduce a shoot-through state without damaging semiconductor devices. When the inverter bridge is in shot-through mode, the front-end diode D is reverse biased with its blocking-voltage expression and other state equations written as follows[6]-[13].

Shoot through ($S_{X=}$ $S_{X,}$ X=A, B, OR; C, D=OFF)

$V_L=V_C+V_{dc}/2$, $V_i=0$

$V_d=V_D=-2V_C$(14)

$I_L=-I_C$, $I_i=I_L-I_C, I_{dc}=0$

Alternatively, when in non-shoot- through active or null state current flows from Z-Source network through the inverter topology to connect ac load during time interval T_1.The expression for non-shoot through is written as,

Non shoot –through ($S_{X\neq}$ $S_{X,\ X=}$A, B, OR C; D=ON)

$V_L= V_{dc}/2 - V_C V_i =2V_C$

$V_{d=}V_D=0$ (15)

$I_{dc}=I_L+ I_C$

$I_{dc}\neq0$ (16)

Performing state-space averaging on (14) and (15) then results obtained from the following expressions which are derived for the calculation of capacitive voltage *VC*, peak dc-link voltage *VP*, and peak ac output voltage Va.

$V_c=\frac{V_{dc}/2}{1-2T0/T}$ (17)

$V_p=\frac{V_{dc}}{1-T_0/T}$ (18)

$V_{ac}=M\frac{V_p}{2}$ (19)

WhereT_0/T*refers* to the shoot-through ratio (T_0/T <0.5) for a single switching period, *M* denotes the modulation index that is used for traditional inverter control, and B = $1/(1-2T_0/T)$ is the boost factor. Clearly, the term in the expression for V_{ac} represents the output amplitude produced by a traditional VSI, which can be boosted by raising *B* above unity and adjusting *M* accordingly[13]. Embedded Z source inverter produce the same gain even though the Embedded Source inverter has dc source embedded within the impedance network for achieving inherent filtering. Observing carefully, a second advantage is also noted in when comparing its capacitive voltage V_C with Z source inverter [8]-[6]. Inferring that second advantage introduced by embedding the source is a significant reduction of the capacitor sizing (voltage rating).The reduction is as much as 50%under nominal condition during which M is set close to unity**.** Although the Embedded Z-source inverter shown in fig (3)uses two independent dc sources to produce balanced front-end impedance in the network but in practice, it is not required for both the sources to be balanced at all. In extreme cases, one or more sources can be omitted. The elimination of one source is a very favorable aspect to the industry, where locating a single source is definitely much easier. The omission of one source is in principle favorable to the industry, where locating a single source is definitely much easier. Relevant mathematical analysis and experimental testing for the case of only a single source powering the EZ-source inverter have already been presented by the authors in [10], where it is generally concluded that a single source is sufficient, if unbalanced voltage drops across the front-end passive *LC* elements are acceptable. In addition to [10], the same analysis can also be found in [11] and [12], which in principle are independent research papers reporting on the same topic and printed at about the same time in the same conferences.The extent of compensation achieved by the described technique is likely to be affected by parasitic components found in a real design, which is beyond the scope of this paper and therefore left for a future investigation.

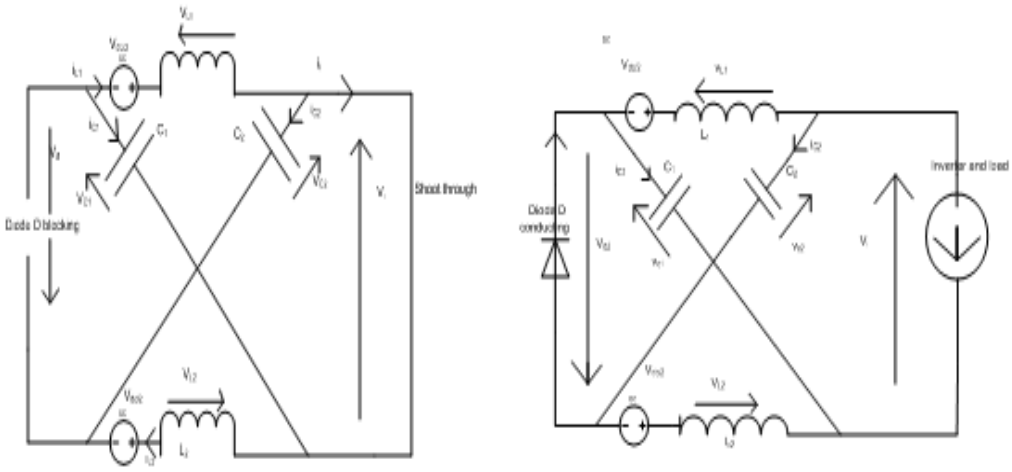

Fig.3 (a) Fig.3 (b)

Fig.3: Equivalent circuit of Embedded Source inverter (a) shoot through state (b) nonshoot-through state.

IV. RESULTS AND DICSSSIONS

This circuit also provides reduced line current harmonics With an EZ-source network constructed using L = 3.3mH, C = 2800 μF, and $V_{dc} \approx$ 100 V and connected to inverter the relevant waveforms obtained by setting the relevant control parameters to $M = 1.15 \times 0.7$ and $T_0/T = 0$ for no shoot-through state insertion .From the fig 4, it is obvious that the output current is sinusoidal, and the measured line-voltage pulse height produced by the inverter, which corresponds to its dc-link voltage of v_i, matches the unboosted theoretical value of ≈100 V calculated using (4). Next, with M kept constant and a shoot-through duration of T_0/T = 0.3 added to the inverter-state

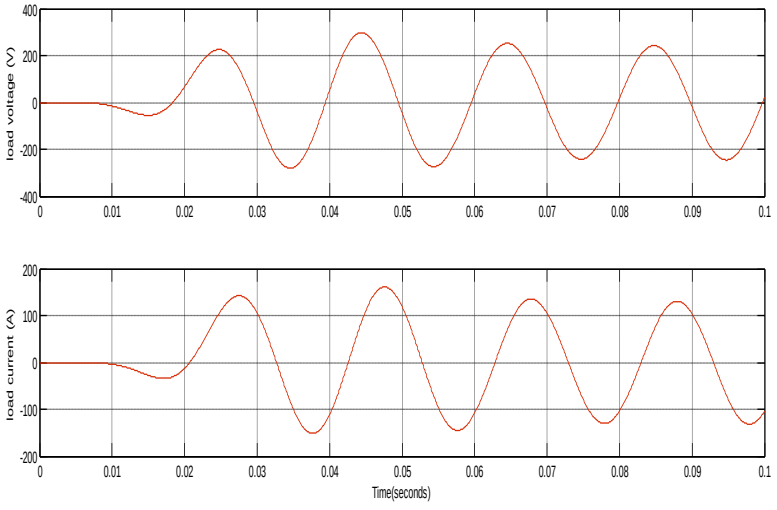

Fig.4: Load voltage and load current

Here sinusoidal waveform of voltage across the load is obtained, peak values being 300V. The current through load is Sinusoidal and the peak value of current is 150 A, as demanded by the load. Due to unexcited EZ-network components, (L1, L2, C1 and C2) in theZ-source inverter took 0.5 seconds to reach at steady state.

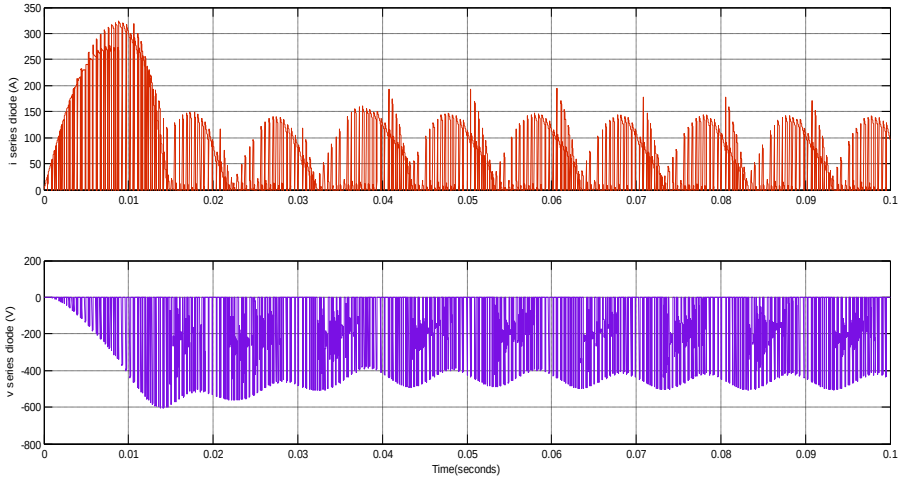

Fig.5: Current and voltage through series diode

The input current passing through the series diode and input voltage that appears across the series diode is shown in fig (5).

V. CONCLUSION

The analysis and simulation of embedded z source H Bridge has been done.The graphplotted in experimental results verified that the boosting of output voltage can be done upto to any value irrespective of input voltage by using E- Sourceinverter. By doing slight modification in the circuitan alternative family of dc-link EZ-source inverters can also be implemented with an even lower network capacitive voltage attained at the expense of no inherent inductive filtering, a noisier source current waveform even under no voltage boosting condition, and the presence of a small negative capacitive voltage. These advantages are obtained with no degradation in gain, diode blocking voltage, and other characteristic properties of the X-shaped impedance network for the same specified shoot-through duration. The practicality of the new Embedded Z-source inverters has been proved by performing and experimentally testing the inverter. Needless to say, in current type inverter also we can apply this embedded concepts.

REFRENCES

[1] Ali,U,andShajith and Kamaraj, "A modified space vector PWM for Bi- directional Z-source inverter", International Conference on Emerging Trends in Electrical and Computer Technology pp. 342-34,(2011).

[2] B. Farhangi and S. Farhangi, "Comparison of Z-Source Inverter and Boost-Buck Inverter Topologies as a single phase transformer-less Photovoltaic Grid- Connected Power Conditioner",IEEE Power Electronics Specialist Conference pp. 74-792006.(2006).

[3] Bakar, M. S., Rahim, N. A. and Ghazali, K. H, "Analysis of various PWM controls on single-phase Z-source inverter".), IEEE Student Conference on Research and Development (SCOReD) pp. 448-451, (2010).

[4] **P**. Loh, D. M. Vilathgamuwa, Y. S. Lai, G. T. Chua and Y. Li,"Pulse-Width Modulation of Z-Source Inverters". IEEE Transactions on Power Electronics vol. 20, no. 6, pp. 1346-1355(2005).

[5] Chandrasekhar, T. and Veerachary, M. "Control of single-phase Z-source inverter for a grid connected system", International Conference on Power Systems pp. 1-6. (2009).

[6] Poh Chiang Loh, Feng Gao,andFredeBlaabjerg, "Embedded EZ-Source Inverter" Industry Applications Society Annual Meeting, Edmonton, AB, Canada, October 5–9, and approved for publication in the IEEE TRANSACTIONS ON INDUSTRY APPLICATIONS(2008).

[7] F. Z. Peng, M. Shen, and K. Holland, "Application of Z-source inverter for traction drive of fuel cell—Battery hybrid electric vehicles,IEEE Transactions on Power Electronics vol. 22, no. 3, pp. 1054–1061, (2007).

[8] Zhiqiang Gao, Ke Shen, Jianze Wang and Qichao Chen, "An Improved Control Method for Inductive Load of Z-Source Inverter", pp.1-4, March 28-31, Asia-Pacific Power and Energy Engineering Conference (APPEEC)(2010).

[9] Y. H. Kim, H. W. Moon, S. H. Kim, E. J. Cheong, and C. Y. Won, "A fuel cell system with Z-source inverters and ultra-capacitors",in Proc. IPEMC, pp. 1587–1591(2004).

[10] F.Gao, P. C. Loh, F. Blaabjerg, and C. J. Gajanayake, "Operational analysis and comparative evaluation of embedded Z-source inverters," in *Proc. IEEE PESC*, 2008, pp. 2757–2763.

[11] **J** Anderson and F. Z. Peng, "Four quasi-Z-source inverters," in *Proc. IEEE PESC*, 2008, pp. 2743–2749.

[12] J. Anderson and F. Z. Peng, "A class of quasi-Z-source inverters," in *Conf. Rec. IEEE IAS* Annu. Meeting, 2008, pp. 1–7**.**

[13] P.Kannan,"Harmonics Analysis and Design of Embedded Z Source inverter for Induction Motor Drive" in January 30(2014).