A COMPLETE ANALYSIS AND DYNAMIC SIMULATIONS OF SUPERCONDUCTING LOGIC GATES

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ABSTRACT

A thorough investigation has been made to obtain SQUID device parameters and properties, and the optimization of the latter for the application of logics gates. SQUID OR, AND gates have been designed theoretically using the optimized techniques. Our concept of turn-on delay has been applied for critically ascertaining the switching speed of these logic gates. The dynamic response of the logics gates have been obtained by computer-simulation. This paper will help for the scientists to have a complete understanding of SQUID logic gates before they are fabricated experimentally to obtain better results. Further, *in this paper a thorough investigation of resistive logic gates such as JAWS, DCI and RCJL has been made. The current equations of each gate at each stage have been deduced. The dynamic response of these gates have been obtained by the computer-simulation. The concept of turn-on delay has been introduced. The effect of overdrive current on turn-on delay for resistive logic gates has been shown. This will provide a better understanding of switching dynamics of the logic gates. Further, we have shown the effect of overdrive current on these logic gates. This paper will help scientists and researchers to have complete understanding of superconducting logic gates before they are fabricated experimentally to obtain optimum results.*

Keywords: Josephson Junction, Superconducting Logic Gates, Computer-Simulation

I. INTRODUCTION

Josephson junction alone cannot be used as a logic gate since it lacks isolation, i.e., the output signal can propagate in the input as well as in the output branches, whereas for logic operation the signal must propagate only in the output branches. The other problem with this circuit is that the output current is not sufficient to switch more than one load. High-gain Josephson logic devices are desired for many reasons: first, they provide higher fan-out capability (fan-out means the number of loads). Second, high-gain to some extent can be traded off to improve the circuit tolerances from variations in processing parameters such as critical currents.

Finally, high-gain would result in shorter gate delays because of the shorter turn-on delays [1]-[4] and the shorter time required for signal currents to reach the device threshold. In practice, a gain of 3 is found to be optimum for Josephson logic circuits. At gains much larger than 3, there is no significant improvements in the gate delay but, on the other hand, the noise margins for the "0" state degrades considerably.

The Superconducting Quantum Interference Device (SQUID) is a device which can be used for both logic and memory applications. It consists of two Josephson junctions coupled by two inductors. The two most attractive features of SQUID devices for logic applications are isolation and serially connected fan-out. The isolation is provided by the transformer coupling between the SQUID and the input. The other advantage of

SQUID is the serial fan-out capability whereby the control lines of many load devices can be connected in series with a single output line. Before fabricating DC SQUD as a logic and memory device, it is very much necessary to have a thorough understanding and optimization of the device for better results. Earlier I have made an attempt to design DC SQUID as a memory device using computer -simulation method [5]. Since the present paper deals with the design of logic gates using the SQUID, it is necessary to have a detailed information regarding the parameters, properties and their optimization for the application of logic and memory cell. In fact, in the present paper we have made an attempt on this line. Two attractive features of SQUID devices for logic applications are isolation and serially connected fan-out. The isolation is provided by the transformer coupling between the SQUID and the input. The isolation is not perfect in the sense that a noise pulse (typically 5 percent) is fed back into the control line when the SQUID switches to the non-zero voltage. The other advantage is the serial fan-out capability by which the control lines of many load devices can be connected in series with a single output line. The main drawbacks of SQUID devices for logic application are relatively large device area and high sensitivity to stray magnetic fields. In SQUID 80% of the area is occupied by the transformer [1]. Further, the high sensitivity to stray magnetic field requires that the SQUID based logic circuits be well shielded from the stray magnetic fields. The resistive logic gates such as JAWS (Josephson Auto-Weber System) [6], DCI (Direct Coupled Isolation) [7] and RCJL (Resistor Coupled Josephson Logic) [8] are chosen because the gate logic delay in this case would consist of the turn-on delay, switching delay and propagation delay, but not the crossing delay as in the case of magnetically coupled logic gates. Further, these resistive logic gates do not have a factor of limiting the size very seriously. So, the gate propagation delay can be made sufficiently small. Therefore, the small time constant of the Josephson junction can be directly attained to these gates. It has been considered by the earlier workers that the turn-on delay of a logic gate is the time taken for the logic gate to obtain 2% of the output current to the load. This consideration seems to be arbitrary.

Due to this fact, in the present paper we have made a thorough investigation of the resistive logic gates. Our concept of turn-on delay has been introduced which will be able to remove the confusion in critically ascertaining the switching speed of these logic gates. Further, the effect of overdrive current on these resistive logic gates has been studied.

II. BRIEF THEORY OF DC SQUID

The Superconducting Quantum Interference Device (SQUID) is a device which can be used for both logic and memory applications. It consists of two Josephson junctions coupled by two inductors as shown in Fig.1a The two most attractive features of SQUID devices for logic applications are isolation and serially connected fan-out. The isolation is provided by the transformer coupling between the SQUID and the input. The other advantage of SQUID is the serial fan-out capability whereby the control lines of many load devices can be connected in series with a single output line. An equivalent circuit of SQUID [9] is shown in Fig.2a. When the Josephson junction A and B are assumed to be point junctions, the maximum Josephson current ratio of the junctions A and B is $a = I_a/I_b > 1$. The total inductance between the junctions is $L = L_1 + L_2$. The insertion point of the gate current I_g is given by the tap ratio, $p = L_1/L$. The control current I_c represents a transformed control current I_c' of a separate control line. The total flux in the interferometer is an integer multiple N of one flux quantum ϕ_o=2.07 mVps. Flux quantum states (FQS) exist within limited range in the current plane I_g, I_c. Their threshold curves are as functions of phase differences across the junctions θ_a and θ_b:

$$I_g = (a.\sin\theta_a + \sin\theta_b) . I_b \quad \text{---------- (1a)}$$

$Ic = [(\theta_a - \theta_b + 2\pi N) / \lambda - (1 - p).\sin\theta_b + p.a \sin\theta_a].I_{b---}$ (1b)

$$\theta_b = arc\cos\left(\frac{-a\cos\theta_a}{1+\lambda a\cos\theta_a}\right); a = I_a / I_b ; L = L_1 + L_2$$

$p = L_1 / L$; $\lambda = 2\pi L. I_b / \phi_o$

The curves depend on five magnitude parameters

The characteristic phase $\lambda = 2\pi L\ I_b/\phi_o$. The maximum Josephson current of the smaller junction I_o

The current ratio, a

The tap ratio, p

The number of flux quanta N.

An example of two FQS in the normalized current plane with $i_G = I_g/I_o$ and $i_C = I_c/I_o$ is given in Fig.3b, for $\lambda = \pi$, a=8, p=0.25 and N=0, 1 [9].

For N = 0 mode, the points A and C are point symmetric with respect to the origin. The same is true for the points B and D. The currents at the points are given analytically [9].

A) $I_{gA} = (a+1)\ I_o$

$I_{cA} = (p.(a+1) - 1).\ I_o$

B) $I_{gB} = (a-1)\ I_o$

$I_{cB}\ (\pi/\lambda + p.(a-1) + 1)\ I_o$

The control current shift is given by [9]

$\Delta I_c = \phi_o / (L_1 + L_2)$

which can also can be written as

$\Delta I_c = 2\pi\ I_o/\lambda$

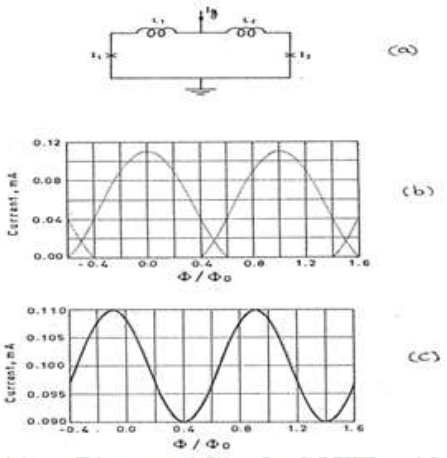

Fig. 1 (a) Diagram of a dc SQUID with bias current. The inductances and junctions on the two sides may be different. The crosses represent the junctions, including resistances and capacitances. (b) The positive half of the threshold characteristic of a symmetric dc SQUID having $L_1 = L_2 = 2.0$ pH and $I_1 = I_2 = 55$ μA.(c) The positive portion of the threshold characteristic of an asymmetric dc SQUID with $L_1 = L_2 = 2.0$ pH and $I_1 = 100$μA ; $I_2 = 10$μA.

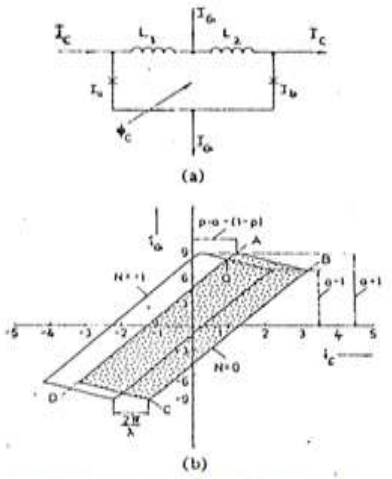

Fig. 2 dc SQUID with two Josephson junctions A and B the total inductance $L = L_1 + L_2$ (a) Equivalent circuit with gate current I_G and the control current I_C. (b) Threshold curves of flux quantum states $I_G = I_G / I_b$ versus $I_C = I_C / I_b$ for a = 8.0, $\lambda = 2\pi$, $p = L_1 / L = 0.25$ and N = -1, 0.

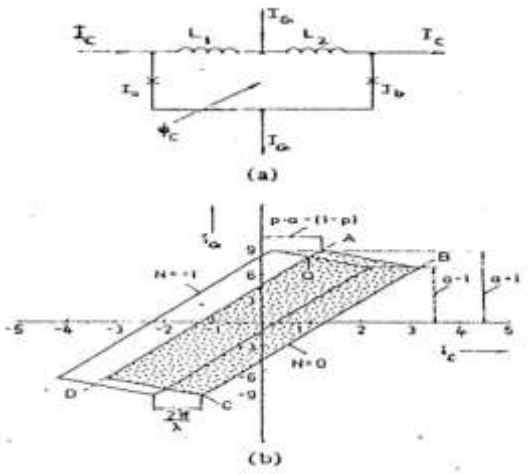

Fig. 3 dc SQUID with two Josephson junctions A and B the total inductance $L = L_1 + L_2$ (a) Equivalent circuit with gate current I_G and the control current I_C. (b) Threshold curves of flux quantum states $I_G = I_G / I_b$ versus $I_C = I_C / I_b$ for a = 8.0, $\lambda = 2\pi$, $p = L_1 / L = 0.25$ and N = -1, 0.

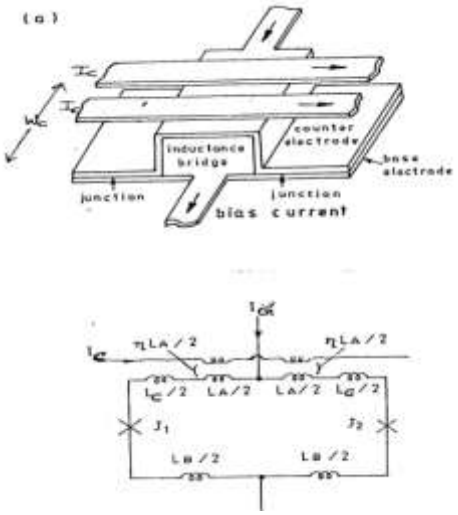

Fig. 3 SQUID and its Equivalent circuit of as a SQUID OR gate

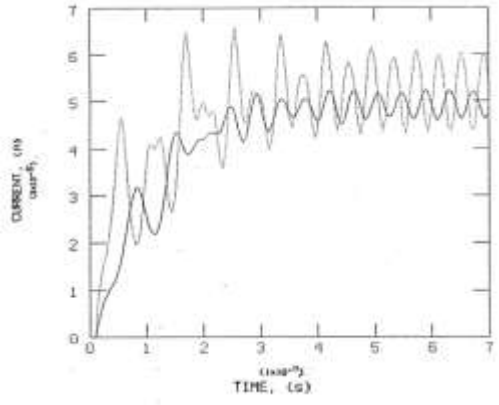

Fig. 4 Dynamic response of a SQUID OR gate using two different technologies. The solid curve shows the output current of Pb-alloy based OR gate with time, whereas the dotted curve indicates the output current variation with time for Nb/A10x/Nb based OR gate

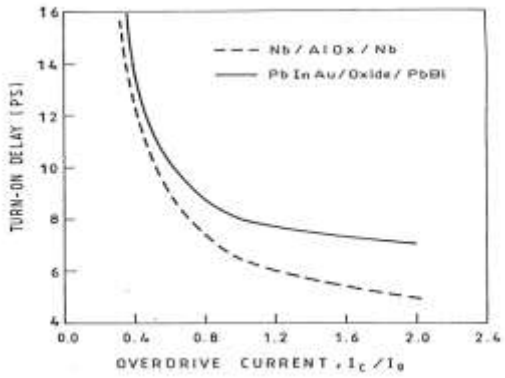

Fig. 5 The turn-on delay of a SQUID OR gate depedance on overdrive current. The solid curve indicates the turn-on delay vs overdrive for a Pb-alloy based OR gate, whereas the dotted curve shows the turn-on delay vs overdrive for a Nb/A10x/Nb based OR gate.

2.1 Dynamic Response of the SQUID

In designing Josephson digital circuits, computer simulations of the static as well as of the dynamic device behaviour play an essential role because of the lack of sufficiently accurate analytical approximations.

The dynamic description of the superconducting networks, containing Josephson tunnel junctions, self- and mutual -inductances, capacitances and resistors, results in a set of equations for the current continuity and zero-voltage sum and the particular current-voltage integral equations of the junctions. IBM and Bell Labs have been adopting the standard electrical network

analysis programs (for examples ASTAP [10], SPICE [11], etc) in order to obtain the circuit static as well as the dynamic response [9].

In the present case we have adopted a more general approach to obtain the dynamic response of SQUID. The dynamic equations of the SQUID have been taken and solved numerically by the Runge=Kutta method. In the switching dynamics of a logic gate, the high-frequency oscillation present in the load current with oscillation periods of a few ps stems from the oscillating supercurrent in the interferometer junctions. The frequency of these oscillations is related by to the actual junction voltage. Because these oscillations are still slow enough and can have sufficient energy to switch the following gate, they have to be modelled accurately although the overall switching transient is in the tenths of ps. For an accurate computation of this oscillation, a minimum time-step size in the simulation of about 0.01 has to be used [12].

From Eqns.(10a) and (10b) we can have,

$(1 - P)I_G + I_C = [(\theta_a - \theta_b + 2\pi N)I_o/\lambda + a\, I_o \sin\theta_a]$

In the dynamic case the above equation modifies to:

$$(1 - P)I_G + I_C = (\theta_a - \theta_b + 2\pi N)\, I_o/\lambda + a\, I_o \sin\theta_a + a\, \frac{\phi_o}{2\pi} C_j \frac{d^2\theta_a}{dt^2} + a\, \frac{\phi_o}{2\pi R_a} \frac{d\theta_a}{dt}$$

$$or\ \frac{d^2\theta_a}{dt^2} = \frac{2\pi}{\phi_o C_j a} [\, (1-p) I_G + I_C + (\frac{\theta_a - \theta_b - 2\pi N}{\lambda})\, I_o \quad - a\, I_o \sin\theta_a - \frac{a\, \phi_o}{2\pi R_a} \frac{d\theta_a}{dt} \quad \text{------ (2)}$$

Similarly,

$$\frac{d^2\theta_b}{dt^2} = \frac{2\pi}{\phi_o\, C_j\, b} [\, pI_G - I_C + (\frac{\theta_a - \theta_b + 2\pi N}{\lambda})\, I_o + b\, I_o \sin\theta_b - \frac{b\, \phi_o}{2\pi\, R_b} \frac{d\theta_b}{dt} \quad \text{--------- (3)}$$

Eqns. (2) and (3) are in the form of the second order differential equation. These equations can be solved by fourth – order Runge-Kutta method on a computer to obtain the dynamic response of the SQUID.

III. SQUID AS AN OR GATE

The basic structure of SQUID OR gate is shown in Fig. 6a and its equivalent circuit is given in Fig. 6b. The SQUID OR gate consists of a 2-junction bridge. In designing the SQUID OR gate, it is necessary to obtain threshold characteristic as a function of various device dimensions. The threshold characteristic is calculated by solving equations derived from the equivalent circuits (shown Fig.6b).

In the calculation, estimated values of inductances in the equivalent circuit play a key role. According to Suzuki [13] the inductances L_A, L_B and L_C are given by

$L_A = \mu_o [(d_{12} + \lambda_{eff})^1 + \lambda_{eff} l_J]/K Wc$

$L_B = \mu_o \lambda_B (1 + l_j)/[K Wc \sinh (d_B/\lambda_B)]$ (4)

$L_C = \mu_o \lambda_C (1 + l_j)/[K Wc \sinh(d_C/\lambda_C)]$

where l is the bridge length, l_J is the junction length, Wc is the counter electrode width,

d_{12} is the thickness of the insulating layer, K is the fringing factor calculated by given [10], d and dC are the base and counter electrode respectively, and u_o is the permeability.

Here λeff is the sum of the effective London penetration depth of both electrodes, and is given by

$\lambda_{eff} = \lambda_B \tanh (d_B/2 \lambda_B) + \lambda_C \tanh (d_C/2 \lambda_C)$

The loop inductance L_{loop} is the sum of L_A, L_B and L_C, and is given by

$L_{loop} = L_A + L_B + L_C = \mu_o [(d_{12} + \lambda loop) 1 + \lambda loop\ l_J]/K Wc$ and

$\lambda_{1oop} = \lambda_B \coth (d_B/\lambda_B) + \lambda_C \coth (d_C/\lambda_C)$

(K, fringing factor, approximately equal to $(1 + 4\ d_{12}/W)$ where $.W > > d_{12}$) For a 2.5 μm Josephson junction technology, the material parameters used for designing the SQUID OR gate .

Further, the SQUID OR gate is designed under the following conditions:

Line width and line spacing = 2μm

Layer-to-Layer registration = 1.5μm.

With Wc = 7.0μm the device area of the SQUID OR gate is 7μm x 16.5μm. $p = L_1/L = 0.5$ and $\lambda = 1.01\ \pi$ (approximately).

Dynamic response:

The dynamic response of the designed SQUID OR gate is obtained by substituting the values of device parameters in Eqns. (2) and (3) and solving them by using the fourth-order Runge-Kutta method on a computer.

In Fig.4 the dynamic response of the designed SQUID OR gate has been obtained for two different technologies. The solid curve shows the output current (load) variation of the SQUID OR gate with time using Pb-alloy technology whereas the dotted curve is obtained from Nb/A10 x/Nb Josephson junction base SQUID OR gate. It is apparent from the simulation that the Nb/A10x/Nb base SQUID OR gate has better features over Pb-alloy based OR gate.

Using our concept of the turn-on delay of the Josephson junction [14], the turn-on delay of the SQUID OR gate has been obtained. We have considered the turn-on delay of the SQUID as the time needed for the output phase of the SQUID to reach its phase $\pi/2$.

In Fig.5, we have shown the turn-on delay of a SQUID logic gate dependence on the overdrive current. The solid curve indicates the turn-on delay vs overdrive curve for a Pb-ally based SQUID OR gate, whereas the dotted curve is the turn-on delay vs time one for a Nb/A10x/Nb based SQUID OR gate. It cane be observed from the figure that the turn-on delay for a Pb-alloy based SQUID OR gate is higher than the Nb/A10 x/Nb based OR gate. This because of the low junction capacitance (0.37pF) in the case of Nb/A10x/Nb based OR gate.

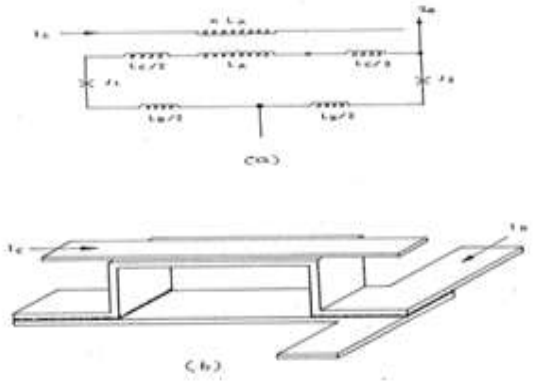

Fig. 7 (a) Equivalent circuit of a SQUID AND gate. b) Static characteristic of the SQUID AND gate. The parameters used for plotting are a = 1.0, b = 3.0, $\lambda = 0.87\pi$ and $p = L_1 / L = 1.0$

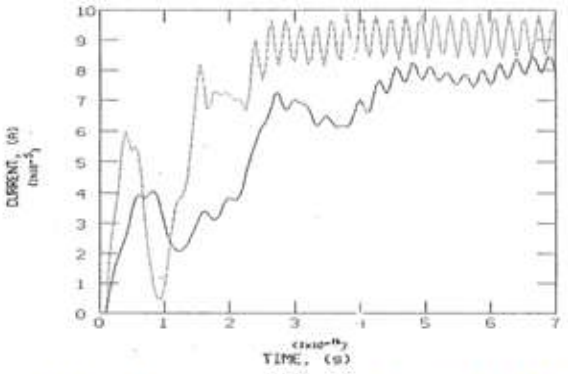

Fig. 8 Dynamic response of a SQUID AND gate using two different technologies. The solid curve shows the output current of Pb-alloy based AND gate with time, whereas the dotted curve indicates the output current variation with time for a Nb/A10x/Nb based AND gate

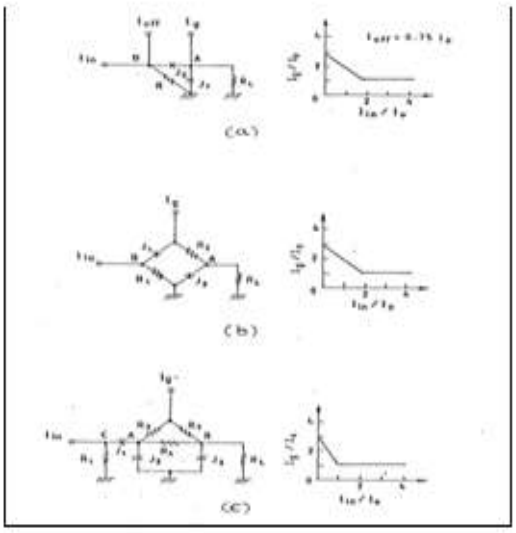

Fig. 9 Circuit configuration of the resistive logic gates with threshold characteristics. (a) JAWS (b) DCI and (c) RCJL

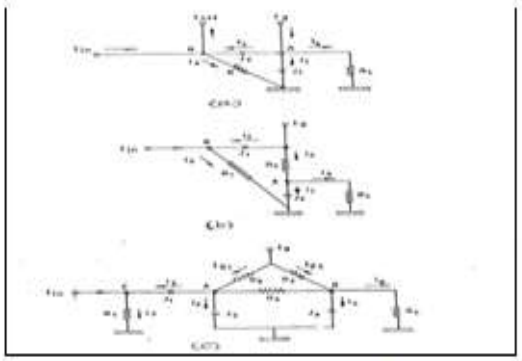

Fig. 10 Circuit configuration of the resistive logic gates with current indication at each stage of the logic gate. (a) JAWS (b) DCI and (c) RCJL.

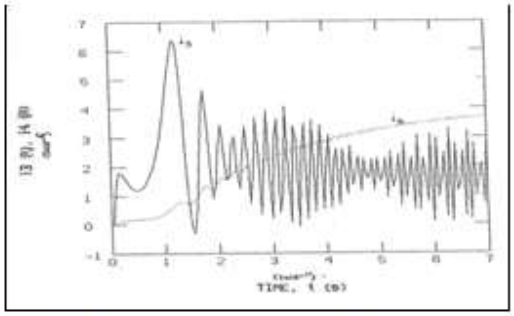

Fig. 11 Simulated switching dynamics of the JAWS gate. Circuit parameters used in the simulation are $I_0 = 0.1$ mA, $C_j = 0.8$ pF, $r = 0.8\Omega$, $r_L = 10\Omega$.

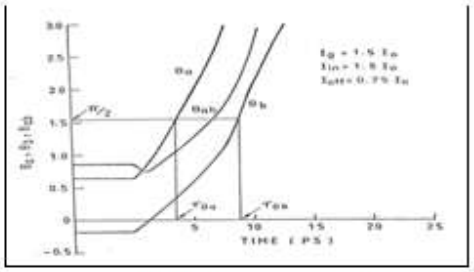

Fig. 12 Simulated phase evolution vs time for a JAWS gate. θ_a and $\theta_a - \theta_b$ are the phase differences of the junctions J_1 and J_2.

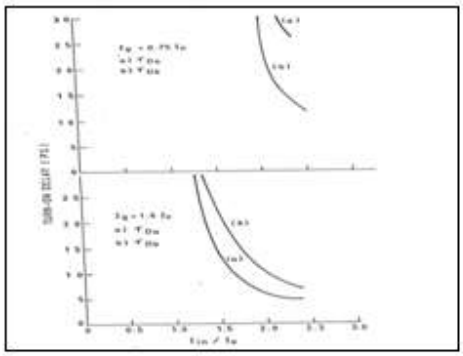

Fig. 13 Turn-on delay of the JAWS gate vs input current. T_{Da} and T_{Db} represent the turn-on delay variation with time at point 'a' and 'b' respectively (as shown in Fig 2a)

IV. SQUID AS AN AND GATE

Asymmetric interferometers with two Josephson junctions or asymmetric dc SQUIDS are very promising devices for digital logic gates. Logic circuits based on these SQUIDS have been investigated [1] [4] . An asymmetric AND interferometer using 3-junctions interferometer have been discussed [15]. In general 3-junction interferometers are used for logic gates whereas 2-junction interferometers are used for the memory application although 3-junction interferometers have better gain tolerances than 2-junction interferometer [16] we have considered 2-junction interferometers for realizing logic gates.

Further, the 2-junction interferometers are simpler and occupy less space compared to 3-junction interferometers. The equivalent circuit of a symmetric two Josephson junction interferometer with nonlinear current injection used for the SQUID AND gate is shown in Fig.6. (according to Beha [9]. The interferometer loop consists of the inductance L = L1 + L2 and the Josephson junctions A and B with the maximum Josephson currents in zero currents in zero field $I_{ja} = a.I_0$ and $I_{jb} = b.I_0$. A and B are the phases differences of the Josephson Junctions A and B. Analytic expressions for the calculation of the boundaries of flux quantum states-are derived as follows: The flux quantization condition and the Kirchhoff law yield for the current i_{CN} and the gate current i_G as follows

$$i_{CN} = \frac{1}{p\lambda}\,[\theta_a - \theta_b - (1-p)\lambda b \sin\theta_b + 2\pi N] \text{ --- (5a)}$$

$$i_G = a \,.\, \sin\theta_a + b.\sin\theta_b - i_{CN} \qquad \text{----- (5b)}$$

$$\lambda = 2\pi\ LI_o / I_o \ ; L = L_1 + L_2 \ ; \ p = L_1 / L$$

Two interferometer as AND gates to achieve the high gain, large slope and wide tolerances, the device parameters are p = 1.0 and λ = 0.87π [16]. In the present case we have tried to achieve these parameters. Beha [17] has investigated a high density SQUID structure for NDRO memory cell. We have used the same structure in order to design AND gate.

. Fig. 7a shows the basic structure of the AND gate and Fig.7b shows its equivalent circuit. It can be observed from the two structures (Fig 7a) that there is only one difference in the current injection. Except this the two structures are identical. The device parameters obtained are similar to SQUID OR gate. The device parameters are p = L_1/L = 1.0 and λ = 1.0 π (approximately) have been obtained .For the SQUID AND gate with Wc = 3.5μm, the area of the gate becomes 3.5μm x 16.5μm. The is a very small dimension of the AND gate.

In Fig.8 the dynamic response of the designed SQUID AND gate has been obtained for two different technologies. The solid curve shows the output current (load) variation of the SQUID AND gate with time using Pb-alloy technology whereas the dotted curve is obtained from Nb/A10x/Nb Josephson junction based SQUID AND gate. It is apparent from the simulation that the Nb/A10 x/Nb base SQUID AND gate has better features over Pb-alloy based AND gate.

V. JAWS (JOSEPHSON AUTO-WEBER SYSTEM)

A gate of this kind has been reported by Fulton, et al [6] and is called JAWS. The basic gate employs two junctions and a resistor as shown in Fig..9 where J_1 and J_2 represent Josephson junctions with critical currents $2I_o$ and I_o and junction capacitances $2C_j$ and C_j respectively. R_L is the load resistor with a resistance r_L. R is the input resistor with a resistance r.

The JAWS gate is biased in the superconducting state by the gate current I_g and the offset current I_{off}. The current levels in J_1 and J_2 are I_g -I_{off} and I_{off}, respectively. When the input signal I_{in} is directly injected to this JAWS device, it will add to the bias current in junction J_1 and subtract from the bias current in junction J_2. The junction J_1 is a current-summing junction which switches first in the gate. This makes J_1 highly resistive, steering most of the signal and the gate current leads to ground through the resistor R. The gate current I_g is selected to be sufficient to then switch J_2 to the non-zero voltage state. With both J_1 and J_2 in the high resistance state, the gate current is steered to the load R and the signal current to ground via the resistor R. The high-resistance of J_2 prevents gate current from feeding back into the input signal line and thus provides isolation.

Fig.10 we have shown the current equations at each stage of the logic gate mentioned. According to Fig.2a, the current equation at each stage can be written as:

$$i_1 = 2\ I_o\ \sin\theta_a + 2\ C_j\ \frac{dV_a}{dt} \quad (1.1)$$

$$i_2 = I_o\ \sin(\theta_a - \theta_b) + C_j\ \frac{d}{dt}(V_a - V_b) \qquad (6.2)$$

$$i_3 = V_b / r \qquad (1.3)$$

$$i_4 = V_a / r_L \qquad (1.4)$$

$$V_a = \frac{\phi_o}{2\pi}\frac{d\theta_a}{dt}\ , V_b = \frac{\phi_o}{2\pi}\frac{d\theta_b}{dt} \qquad (6.5)$$

$$I_g = i_1 + i_2 + i_4 \qquad (6.6)$$

and $I_{in} + i_2 = i_{off} + i_3 \qquad (5.7)$

(Note: Here the effect of subgap quasiparticle resistance R_j has been neglected since $R_j >> r, r_L$).

Dynamic case:

Eqn. (6.1) can be written as

$$i_1 = 2\ I_o\ \sin\theta_a + 2\ C_j\ \frac{d^2\theta_a}{dt^2}\ \frac{I_o}{2\pi}$$

$$or\ \frac{d^2\theta_a}{dt^2} = \frac{\pi}{\phi_o\ C_j}[i_1 - 2\ I_o\ \sin\theta_a] \qquad (6.8)$$

Similarly, Eqn.(1.2) can be written as

$$\frac{d^2\theta_b}{dt^2} = \frac{2\pi}{\phi_o\ C_j}[\frac{i_1}{2} - i_2 - 2I_o\sin\theta_a + I_o\sin(\theta_a - \theta_b)] \qquad (1.9)$$

Further, from Eqns. (6.6) and (6.7) we get, $i_1 = I_g + I_{in} - I_{off} - (i_3 + i_4)$

$$i_2 = I_{off} - I_{in} + i_3$$

Substituting the above values i_I and i_2 in Eqns.(6.8) and (6.9), we obtain,

$$\frac{d^2\theta_a}{dt^2} = \frac{\pi}{\phi_o\ C_j}[i_g + I_{in} - I_{off}$$

$$-2I_o\sin\theta_a\ \frac{\phi_o}{2\ \pi\ r}\ \frac{d\theta_b}{dt} \qquad (6.II)$$

$$-\frac{\phi_o}{2\ \pi\ r_L}\ \frac{d\theta_a}{dt}]$$

$$and\ \frac{d^2\theta_b}{dt^2} = \frac{2\pi}{\phi_o\ C_j}[\frac{i_g}{2} + \frac{3}{2}\ I_{off} + \frac{3}{2}\ I_{in}$$

$$+2I_o\sin\theta_a + I_o\sin(\theta_a - \theta_b)]$$

$$-\frac{3\ \phi_o}{4\ \pi\ r}\ \frac{d\theta_b}{dt} - \frac{\phi_o}{4\ \pi\ r_L}\ \frac{d\theta_a}{dt}] \qquad (6.III)$$

Computer-simulated pulse response of the JAWS gate can be obtained by solving the Eqns.(6.II)and(6.III) for an input current Ii_n applied as a step function at t=0 with amplitude 1.5 I_{th} (threshold current).

In Fig.11 the current variations with time at different stages of the JAWS gate (shown in Fig.10a) have been plotted. The parameters chosen for plotting are I_o = 0.1mA and C_j = 0.8pF. These curves are almost similar to

those obtained by Josephson [5] using computer simulation. This gives confidence to our simulation approach that we have adopted in the present case in order to investigate the switching dynamics of logic gates. Since Nb/A10 x/Nb Josephson technology has better qualities over Pb-alloy technology, we have used Nb/A10 x/Nb Josephson junction parameters for the simulation of the resistive logic gates such as JAW, DCI and RCJL. The parameters are I_o = 87mA and C_j = 0.37pF. It may be pointed out that in estimating the turn-on delay of a logic gate, Sone [5] has considered the time that is needed to reach 2% of the output current to the load.

This consideration seems to be arbitrary. In the present case we have defined turn-on delay of a logic gate in a more critical way using the concept of the turn-on delay of Josephson junction discussed in paper[6]. It is the time taken by the output phase to reach to a value $\pi/2$

The solid curve indicates the current variation (i_3) with time at stage 'b' as shown in Fig.10a and the dotted curve indicates the current i_4 (output current) with time at a stage 'A'. Further, in Fig.12 we have shown the phase variations with time at different stages of the JAWS gate. The biasing and overdrive current conditions are as follows: $I_g = 1.5\ I_o$; $I_{in} =$ 1.5 I_o and $I_{off} = 0.75I_0$. Using our concept of turn-on delay[6], the turn-on delay at each stage of the JAWS gate has been indicated. This will give an exact physical understanding of switching dynamics of the JAWS gate[7].

Also we have plotted (Fig-13) the effect of overdrive current on the turn-on delay of a JAWS gate under different biasng conditions, I_g = 0.75 I_o, 1.5 I_o and 2.25 I_o. In. It can be observed from Fig.7 that the turn-on delay of a JAWS gate decreases with the increase of overdrive current. Also, the turn-on delay decreases with the increase of biasing rate. So by choosing large biasing and overdrive currents we can minimize the turn-on delay of the JAWS gate.

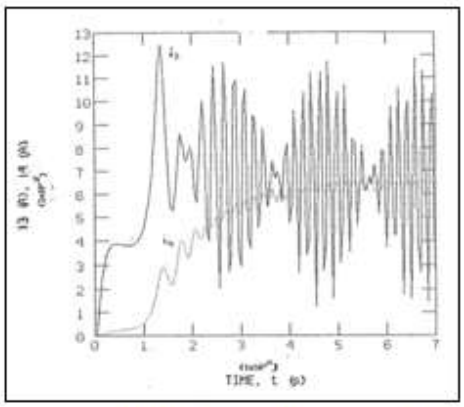

Fig. 14 Simulated switching dynamics of the DCI gate. Circuit parameters used in the simulaton are from Nb/A10x/Nb Josephson technology and are given as I_o = 0.087 mA, C_j = 0.37 pF, $R_1 = R_2$ = 0.8Ω, r_L = 10Ω. The swithching waveforms current flowing in the input resistor R and the output current respectively.

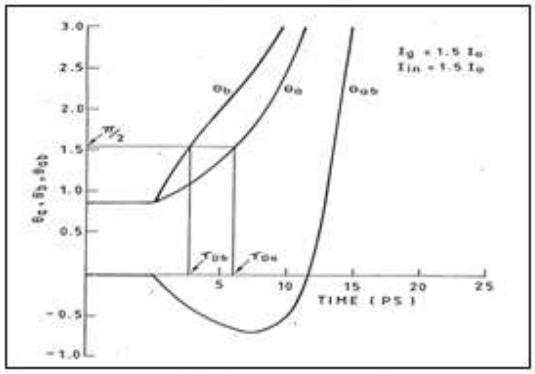

Fig. 15 Simulated phase evolution vs time for a DCI gate. θ_a and θ_{ab} are the phase differences of the junctions J_1 and J_2, respectively. I_o = 0.087 mA, C_j = 0.37 pF, R1 = R_2 = 0.8 Ω and r_L = 10 Ω.

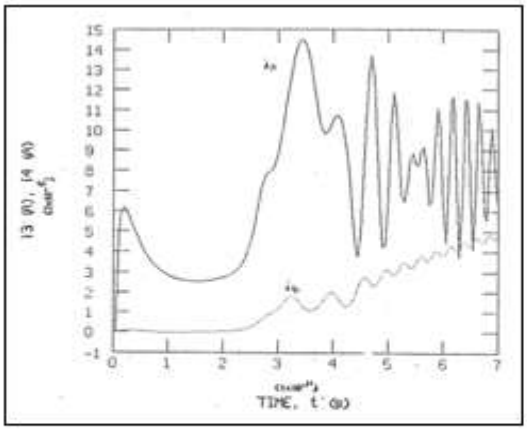

Fig.16 Simulated switching dynamics of the RCJL gate. Circuit parameters used in the simulation are fromNb/A10x/Nb Josephson technology and are given as I_o = 0.087 mA,Cj = 0.37 pF, $R_1 = R_2 = R_3$ = 0.8 Ω, rL = 10 Ω..

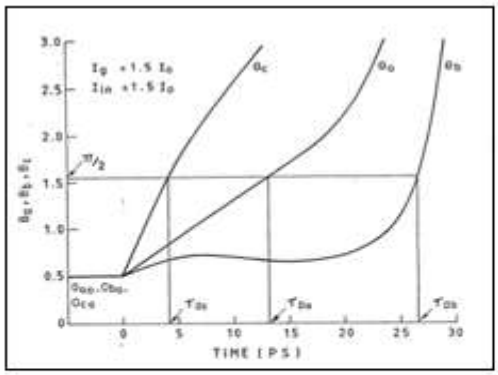

Fig. 17 Simulated phase evolution vs time for a RCJL gate. θa θb and θc are the phase variations at points 'a', 'b' and 'c' respectively. Circuit parameters used in the simulation are I0 = 0.087 Ma Cj = 0.37 pF, $R_1 = R_2 = R_3$ = 0.8 and rL = 10 Ω

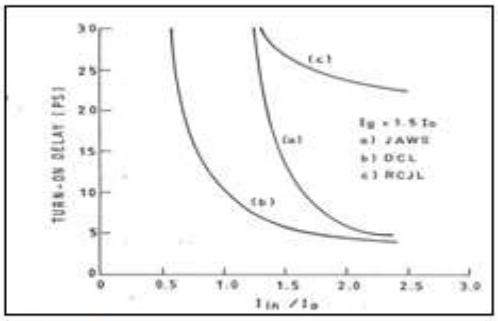

Fig. 18 Turn on delay vs input current of JAWS, DCI and RCJL gate under same biasing condition, Ig = 1.5I_0.

VI. DCI (DIRECT COUPLED ISOLATION)

This was proposed by Gheewala et al [7]. Here the J osephson junction is used just a so called "diode" junction - connecting the input signal to logic device to provide isolation.

It consists of two Josephson junctions J_1 and J_2 as shown in Fig.10b. The junctions J_1 has a critical current I_o and junction capacitance C_j, and the junction J_2 has a critical current 2 I_o and the junction capacitance $2C_j$. The resistances of R_1 and R_2 are r and r/2 respectively. The DCI gate is biased in the superconducting state by the injection of the input current I_{in}. The junction J_2 plays the role of the current-summing junction in this gate.

When the input signal I_{in} is directly injected to this DCI gate, it will add to the bias current in junction J_2 and subtract from the bias in junction J_1. The junction J_2 is a current-summing junction which switches first to non-zero voltage state. This makes J_2 highly resistive, steering most of the signal and the gate current to ground through the resistor R_1 ($R_L >> R_1$). The gate current I_g is selected to be sufficient to then switch J_1 to the non-zero voltage state. With both J_1 and J_2 in the high-resistance state, the gate current is steered to the R_L and signal current to ground via the resistor R_1. The high-resistance of J_1 prevents gate current from feeding back into the input signal line and thus provides isolation. However, the isolation is not perfect and a small amount of current (typically 3-5 percent) is fed back into the input line.

The above DCI gate can be modified or converted to a JAWS gate (as shown Fig.10b). Here two differences are there between DCI and JAWS gates, one is the I_{off} current is absent for DCI gate and the other one is that the extra resistor R_2 is connected in series with the junction J_2.

According to Fig.10b the current equations at each statge of the DCI gate can be written as similar to JAWS gate

Dynamic case: By modifying equations 6.1 to 6.6 we can obtain similar type Eqns.(6.II)and(6.III) for an input current Ii_n applied as a step function at t=0 with amplitude 1.5 I_{th} (threshold current

The dynamic response of the DCI gate at each stage (shown in Fig.14) have been obtained from commputer simulation. The DCI logic gate characterstics are similar to JAWS gate, and have advantages over JAWS in the better margin and gains due to the lack of I_{off} (offset) current In Fig.15 we have shown the phase variations with time at different stages of the DCI gate (shown in Fig.10b). The biasing and overdrive current conditions are as follows: I_g = 1.5 I_o and I_{in} = 1.5 I_o

VII. RCJL (RESISTOR COUPLED JOSEPHSON LOGIC)

The curcuit configuration and the threshold curve for the RCJL gate are shown in Fig.10c. The junctions J_1, J_2 and J_3 have critical currents I_o, 3/2 I_o, and 3/2 I_o, and junction capacitances of C_j, 3/2 C_j, and 3/2 C_j, respectively. The resistor R_2, R_3 and R_4 have the same values of the resistance r' and the resistance of R_1 is r. The RCJL gate is biased in the superconducting state by the injection of the input current I_{in}. The junction J_2 plays a role of the current-summing junction in this gate. The operation of the RCJL gate is as follows:

Initially the gate current I_g splits into I_{gl} and I_{g2} in the inverse ratio of resistors r_2 and r_3. When the input current Iin (I_c) is applied at the node C, the I_{in} goes through the junction J_1 and is injected into the junction J_2. The junction J_2 subsequently switches from the superconducting state to the resistive state. A fraction of the Josephson current having shown in J_2, swings over the junction J_3 through r2, r3, r4, and causes J_3 to switch. Consequently, the gate current I_g is steered towards the junction J_1, and J_1 switching results. After J_1 switching, I_g is steered into the load R_l and I_{in} is terminated through R_l. Gate switching with input-output isolation is completed. In the RCJL gate, total I_{in}current contributes to initialization of the switching sequence, while only a fraction of I_g contributes to it. This results in a high input sensitivity.

According to Fig.2c, the current equations at each stage of the RCJL gate can be written as as similar to JAWS gate:

(b) Dynamic case: By modifying current equations we can obtain similar type Eqns.(6.II)and(6.III) for an input current Ii_n applied as a step function at t=0 with amplitude 1.5 I_{th} (threshold current

Computer-simulated pulse response of the RCJL gate can be obtained by solving the for an input current I_{in} applied as a step function at t=0 with amplitude 1.5 I_{th}

The current variations with time for a RCJL gate at each stage have been plotted in Fig.16 using computer simulation. The parameters used are the same that have been used for JAWS and DCI gates. The solid curve shows the current variation with time at point 'A' (as shown in Fig.10c) and the dotted curve shows the output current variation with time.

In Fig.17 we have shown the phase variations with time at different stages of the RCJL gate using computer simulation. The biasing and overdrive current conditions are as follows: I_g = 1.51_0 and I_{in} 1.51_0. Using our concept of turn-on delay[6], the turn-on delay at each stage of the RCJL gate has- been indicated. This will give an exact physical understanding of switching dynamics of the RCJL logic gate[7].

Finally in Fig.18 we have compared the effect of turn-on delay vs overdrive for JAWS, DCI and RCJL gates under the same biasing condition, $I_g = 1.51_0$. It is observed for the low fan-out (here fan-out is one) the DCI logic gate seems to be a better choice for the logic circuit application because of its low turn-on delay and high-speed performance.

VIII. CONCLUSIONS

In the present paper we have made an attempt to obtain the optimized parameters, properties and optimizations techniques of SQUID to be useful for the design of logics and memory cells. For logic and memory applications, it is found that the optimized device parameters are p = 0.5and $\lambda = \pi$. However, for the SQUID used as an AND gate, the device parameters are obtained as p = 1.0 and $\lambda = \pi$, so that i t provides large gain and operating margins. The logic and memory cell have been designed using these optimized techniques and the dynamic response of these have been obtained by computer-simulation. It is apparent from the simulation that the speed of the designed logic and memory cell is extremely high compared to earlier investigations. Further, the circuit dimension of the logic and memory cell is very low.

A thorough investigation of JAWS, DCI and RCJL logic gates have been made [6][7][8]. The dynamic response of these logic gates are obtained by computer-simulation. The concept of our turn-on delay[14] has been introduced which has helped us in critically ascertaining the switching speed of the logic gates. The effect of turn-on delay on overdrive current has been studied. It is observed that for low fan-outs, the DCI logic gate seems to be a better choice for logic circuit application. It is expected that the concept of turn-on delay will be able to remove confusions which are lying in the earlier investigations.

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