A NOVEL BRIDGELESS SEPIC CONVERTER WITH A RIPPLE FREE INPUT CURRENT

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ABSTRACT

Conventional power factor correction (PFC) single ended primary inductor converter (SEPIC) suffers from high conduction loss at the input bridge diode. To solve this problem, a bridgeless SEPIC converter with ripple-free input current is proposed. In the proposed converter, the input bridge diode is removed and the conduction loss is reduced. In addition, the input current ripple is significantly reduced by utilizing an additional winding of the input inductor and an auxiliary capacitor. Similar to the conventional PFC SEPIC converter, the input current in a switching period is proportional to the input voltage and near unity power is achieved. The operational principles, steady-state analysis, and design equations of the proposed converter are described in detail. Experimental results from a 130W prototype at a constant switching frequency of 100 kHz are presented to verify the performance of the proposed converter.

Index terms: Bridgeless Converter Coupled Inductor, Power Factor Correction (PFC), Single-Ended Primary Inductor Converter (SEPIC).

I INTRODUCTION

According to the demand on high efficiency and low harmonic pollution, the active power factor correction (PFC) circuits are commonly employed in ac–dc converters and switched-mode power supplies. Generally, these kinds of converters include a full-bridge diode rectifier on an input current path so that conduction losses on the full-bridge diode occur and it will be worse especially at the low line. To overcome this problem, bridgeless converters have recently been introduced to reduce or eliminate the full-bridge rectifier, and hence their conduction losses [1]–[13]. A bridgeless boost converter is widely used in advantages of reduced input current ripple, but its output voltage should be higher than the peak voltage of the input voltage [1]–[6]. Relatively low output voltage of PFC converters is required in many applications such as low-voltage switched-mode power supplies. PFC buck converters are more suitable for these applications due to their low output voltage. A bridgeless buck converter was proposed in [7] and [8]. Like conventional PFC buck converters, the output voltage of the converter proposed in [7] and [8] is lower than the peak value of the input voltage.

However, since the input current of the PFC buck converter has dead angles during the time intervals when the input voltage is lower than the output voltage, there is a strong tradeoff between power factor and output voltage selection. On the other hand, a SEPIC PFC converter can provide a high power factor regardless its output voltage due to its step up/down function. In [9]–[13], several bridgeless single-ended primary inductor converters (SEPICs) were

proposed. The efficiency of these converters is improved by removing the input bridge diode. However, bulk input inductor or another LC filter is required to suppress the input current ripple.

In Fig. 1, a bridgeless SEPIC PFC converter suggested in [11] is shown. The component count is reduced and it shows high efficiency due to the absence of the full-bridge diode. However, in this converter, an input inductor with large inductance should be used in order to reduce the input current ripple. In addition, the conduction losses on intrinsic body diodes of the switches are caused by using single pulse width modulation (PWM) gate signal.

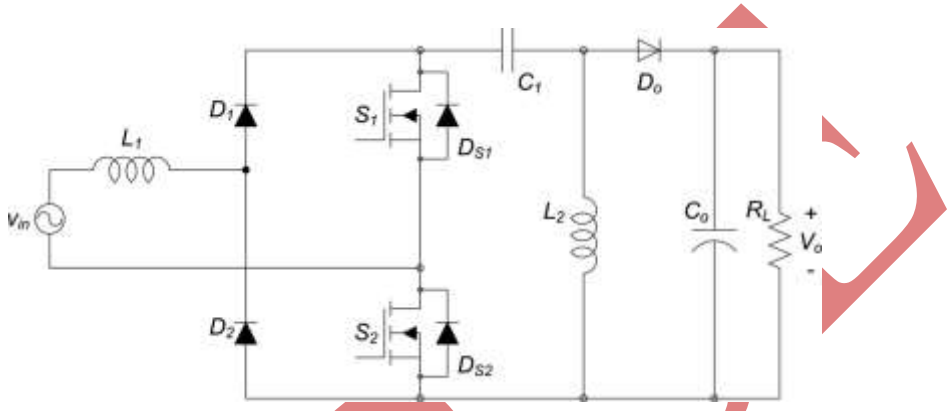


Fig. 1. Bridgeless SEPIC PFC converter

In order to overcome these problems, a bridgeless SEPIC converter with ripple-free input current is proposed in Fig. 2. An auxiliary circuit, which consists of an additional winding of the input inductor, an auxiliary small inductor, and a capacitor, is utilized to reduce the input current ripple. Coupled inductors are often used to reduce current ripple. The shaded area in Fig. 2 represents the auxiliary circuit for achieving the input current ripple cancellation.

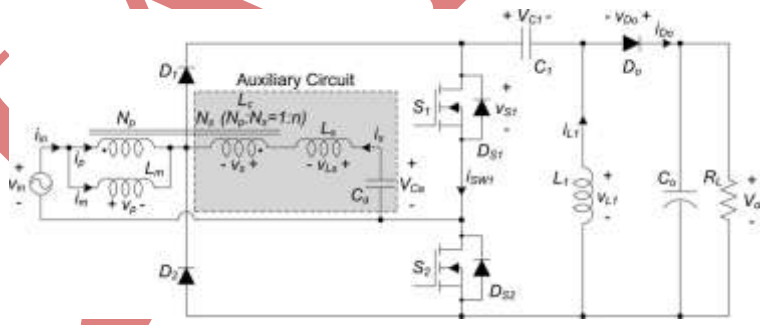


Fig. 2. Proposed Bridgeless SEPIC Converter

Fig. 3 shows the proposed gate signals for the switches. For a half period of the input voltage, one switch is continuously turned ON and the current via an intrinsic body diode is forced to flow through the channel of the switch. It can reduce the conduction loss on the switch further and the efficiency can be improved.

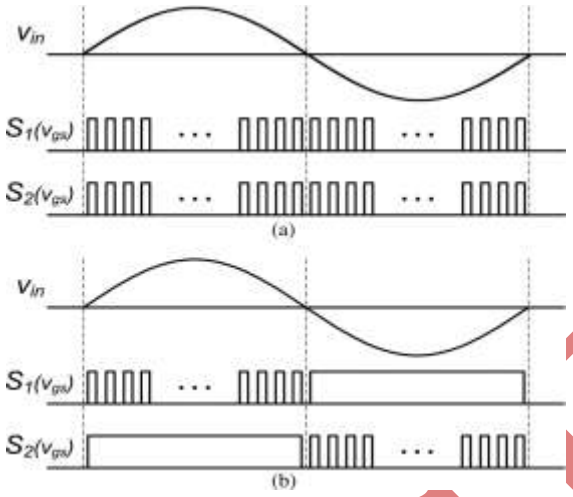
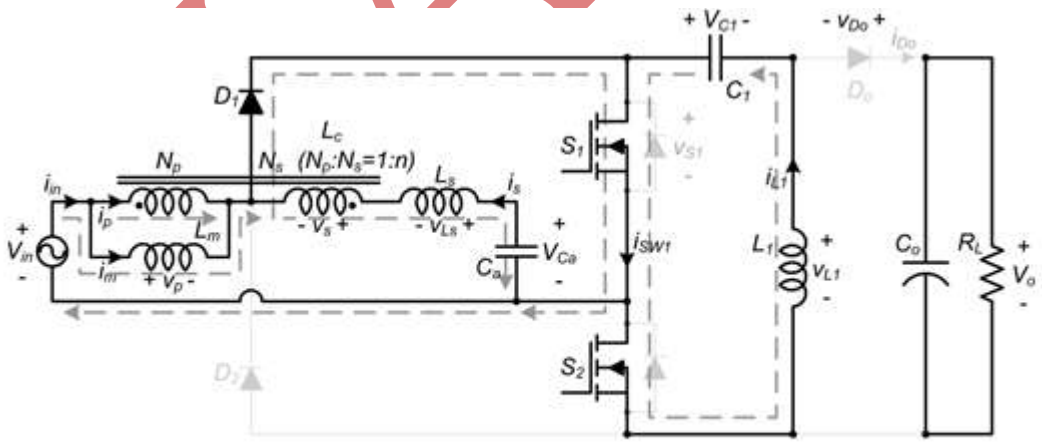


Fig. 3. Gate driving signals. (a) Same gate signals for S1 and S2 (b) Proposed gate signals for S1 and S2

Fig. 2 shows the circuit diagram of the proposed bridgeless SEPIC converter with ripple-free input current. The auxiliary circuit includes an additional winding No of the input inductor Lc an auxiliary inductor L and a capacitor Co. The coupled inductor Lc is modeled as a magnetizing inductance Lm and an ideal transformer which has a turn ration of 1:n. The operation of the proposed converter is symmetrical in two half-line cycles of input voltage. Therefore, the converter operation is analyzed during one switching period in the positive half-line cycle of the input voltage. It is assumed that the converter operates in discontinuous conduction mode (DCM), so the output diode D is turned OFF before the main switch is turned ON. The capacitance of the output capacitor Co is assumed sufficiently large enough to consider the output voltage V as constant.

Fig. 5 shows the operating modes in the positive input voltage. Before t0, the switch S1 and the diode D are turned OFF and the switch S is conducting. The input current is the sum of the freewheeling currents I1 and I2.



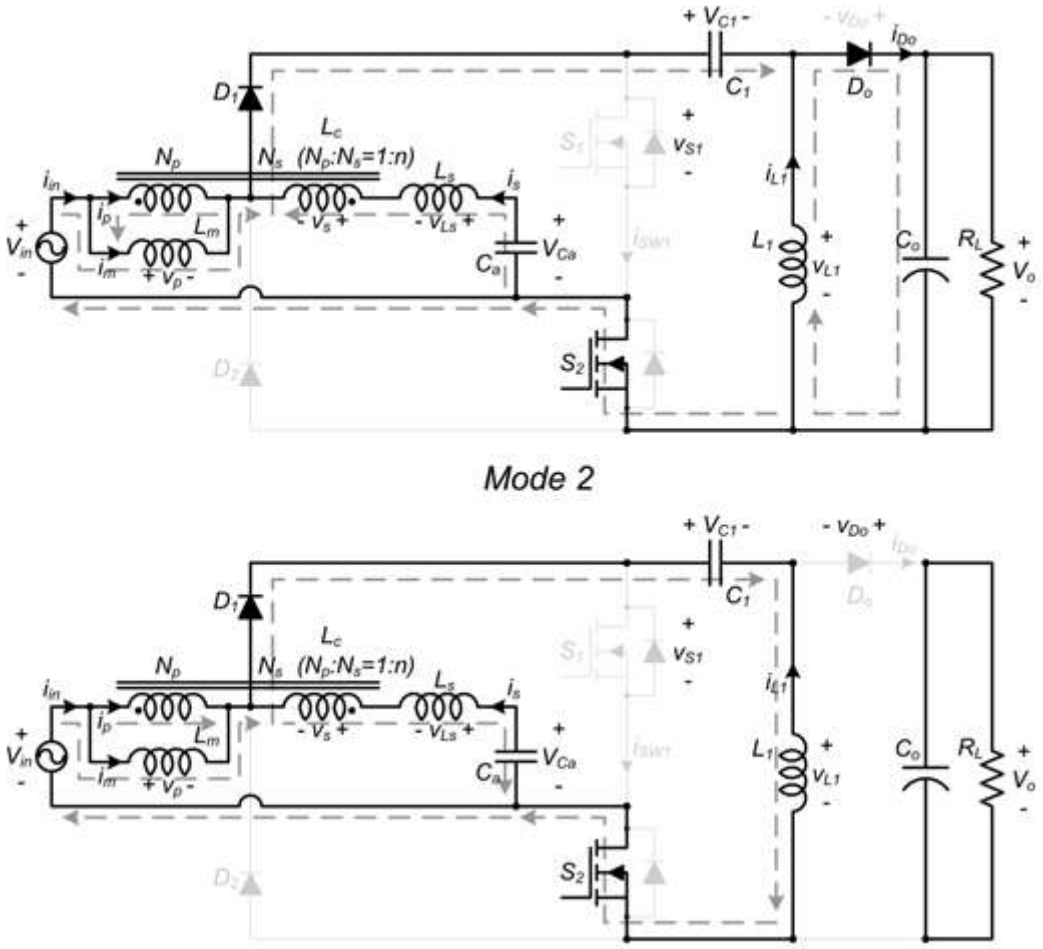


Fig. 5. Operating modes

II SIMULATION RESULTS

The prototype of the proposed converter is implemented with the same specifications of the simulation in order to verify the theoretical analysis and simulation results. The switching devices, IRFPS43N50K for switches and RF2001T3D for all diodes, are used in this converter. The control circuit is implemented with a constant frequency pulse width modulation controller KA7552 from Fairchild. The controller power consumption is not considered in the laboratory prototype. For the magnetic devices, ferrite EI Core EI3329S from SAMHWA Electronics and Litz wire (32/φ0.12) are used.

The input current is a perfect replica of the input voltage and is exactly in phase with that. Fig. 6 shows voltage and current at positive input voltage. It is clear that the input current ripple is completely removed by utilizing a coupled inductor which has a small magnetizing inductance. And because of operating in DCM, the output diode D is turned OFF under zero-current switching condition.

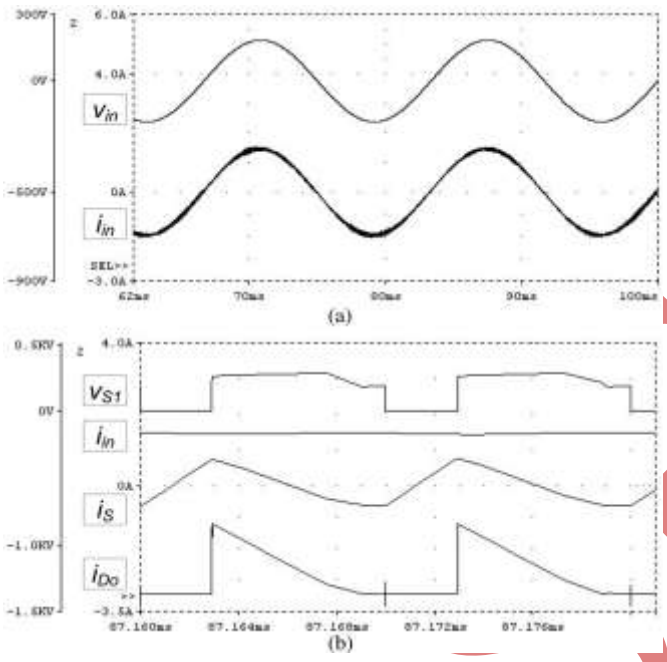


Fig 6: Simulation Results (A) Voltage (B) Current

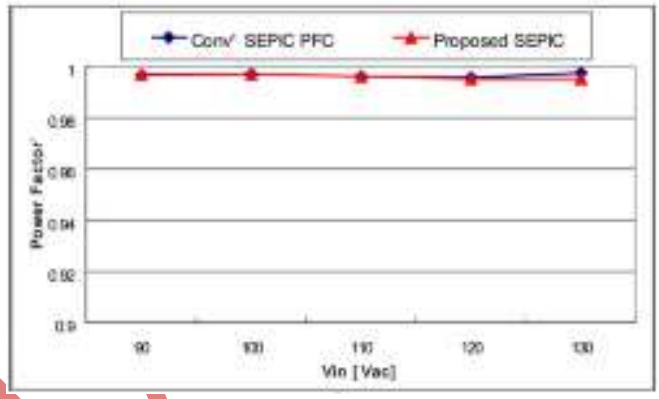


Fig 7: Simulation Results For PFC

III CONCLUSION

A bridgeless SEPIC converter with ripple-free input current has been proposed. In order to improve the efficiency, the input full-bridge diode is eliminated. With the proposed gate driving method, the efficiency is improved by 0.45%. In addition, the input current ripple of the proposed converter is significantly reduced by utilizing an auxiliary circuit consisting of an additional winding of the input inductor, an auxiliary small inductor, and a capacitor. The major disadvantage of the proposed converter is that it has three magnetic components. The theoretical analysis, simulation results, and experimental results were provided.

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