

A STEP-DOWN TRANSFORMER LESS SINGLE STAGE SINGLE-SWITCH AC/DC CONVERTER

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ABSTRACT

This paper presents a step-down transformer less single-stage single-switch ac/dc converter suitable for universal line applications. This topology integrates a Dc to Dc converter power-factor correction (PFC) cell with a buck–boost dc/dc cell and part of the input power is coupled to the output directly after the first power processing. In this paper low output voltage is obtained with a novel method i.e. direct power transfer feature and sharing capacitor voltages, the converter is able to achieve efficient power conversion, high power factor, low voltage stress on intermediate bus and low output voltage without step-down transformer. The absence of transformer reduces the component counts and cost of the converter. Unlike most of the boost-type PFC cell, the main switch of the proposed converter only handles the peak inductor current of dc/dc cell rather than the superposition of both inductor currents. Detailed analysis and design procedures of the proposed circuit are given and verified by experimental results.

I INTRODUCTION

Single-Stage (SS) ac/dc converters have received much attention in the past decades because of its cost effectiveness, compact size, and simple control mechanism. Among existing SS converters, most of them are comprised of a boost power-factor correction (PFC) cell followed by a dc/dc cell for output voltage regulation [1]. Their intermediate bus voltage is usually greater than the line input voltage and easily goes beyond 450 V at high-line application [8]. Although there are a lot of efforts to limit this bus voltage, it is still near or above the peak of the line voltage due to the nature of boost-type PFC cell. With a simple step-down dc/dc cell (i.e. buck or buck–boost converter), extremely narrow duty cycle is needed for the conversion. This leads to poor circuit efficiency and limits the input voltage range for getting better performance [9], [10]. Therefore, a high step-down transformer is usually employed even when galvanic isolation is not mandatory. Hence, non-isolated ac/dc converter can be employed to reduce unnecessary or redundant isolation and enhance efficiency of the overall system. Besides, leakage inductance of the transformer causes high spike on the active switch and lower conversion efficiency. To protect the switch, snubber circuit is usually added resulting in more component counts [13]. In addition, the other drawbacks of the boost-type PFC cell are that it cannot limit the input inrush current and provide output short-circuit protection. Apart from reducing the intermediate bus voltage, the converter in [19] employs resonant technique to further increase the step-down ratio based on a buck converter to eliminate the use of intermediate storage capacitor. The

converter features with zero-current switching to reduce the switching loss. However, without the intermediate storage, the converter cannot provide hold-up time and presents substantial low-frequency ripples on its output voltage. Besides, the duty cycle of the converter for high-line input application is very narrow, i.e., $< 10\%$. This greatly increases the difficulty in its implementation due to the minimum on-time of pulse-width-modulation (PWM) IC and rise/fall time of MOSFET. In this paper, an integrated buck–buck–boost converter with low output voltage is proposed. The converter utilizes a buck converter as a PFC cell.

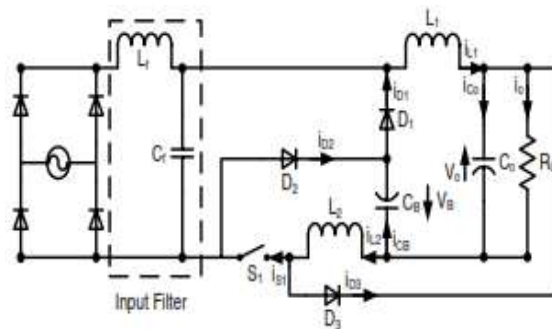


Fig 1: Proposed dc/dc Converter

The figure 1 shows the proposed converter, which consists of the merging of a buck PFC cell (L_1 , S_1 , D_1 , C_o , and C_B) and a buck–boost dc/dc cell (L_2 , S_1 , D_2 , C_o , and C_b) is shown. Moreover, both cells are operated in discontinuous conduction mode (DCM) so there are no currents in both inductors L_1 and L_2 at the beginning of each switching cycle t_0 . Due to the characteristic of buck PFC cell, there are two operating modes in the circuit.

II OPERATION OF THE CONVERTER

Mode A ($V_{in}(\theta) < V_b + V_o$); when the input voltage is smaller than the sum of intermediate bus voltage and output voltage, the buck pfc cell becomes in active and does not shape the line current around zero-crossing line voltage, owing to the reverse biased of the bridge rectifier. Only the buck–boost dc/dc cell sustains all the output power to the load. Therefore, two dead-angle zones are present in a half-line period and no input current is drawn as shown in Fig. 1(b). The circuit operation within a switching period can be divided into three stages and the corresponding sequence is Fig. 2(a),(b), and (f). Fig. 3(a) shows its key current waveforms.

Stage 1: from period d_1T in fig 3(a): when switch S_1 is turned ON, inductor L_2 is charged linearly by the bus voltage V_b while diode D_2 is conducting. Output capacitor C_o delivers power to load.

Stage 2: from period d_2T in fig 3(a): when switch S_1 is turned OFF, diode D_s becomes forward biased and energy stored in L_2 is released to C_o and the load.

Stage 3: from period $d_3T - d_4Ts$ in fig 3(a): The inductor current i_{L2} is totally discharge and only C_o sustains the load current.

Mode B ($V_{in}(\Theta) > V_b + V_o$); This mode occurs when the input voltage is greater than the sum of the bus voltage and output voltage. The circuit operation over a switching period can be divided into four stages and the corresponding sequence is Fig. 2(c), (d), (e), and (f). The key waveforms are shown in Fig. 3(b).

Stage 1: from period $d1T$ in fig 3(b) : when switch S_1 is turned ON, inductor L_2 and L_1 is charged linearly by the bus voltage V_b while diode D_2 is conducting.

Stage 2: from period $d2T$ in fig 3(b): when switch S_1 is turned OFF, inductor current i_{L1} decreases linearly to charge C_b and C_o through D_1 as well as transferring part of the input power to load directly.

Stage 3: from period $d3T - d4Ts$ in fig 3(b): The inductor current i_{L1} continuous to deliver current to C_o and the load until its current reaches zero.

Stage 4: from period $d4Ts$ in fig 3(b): only C_o delivers all the output power.

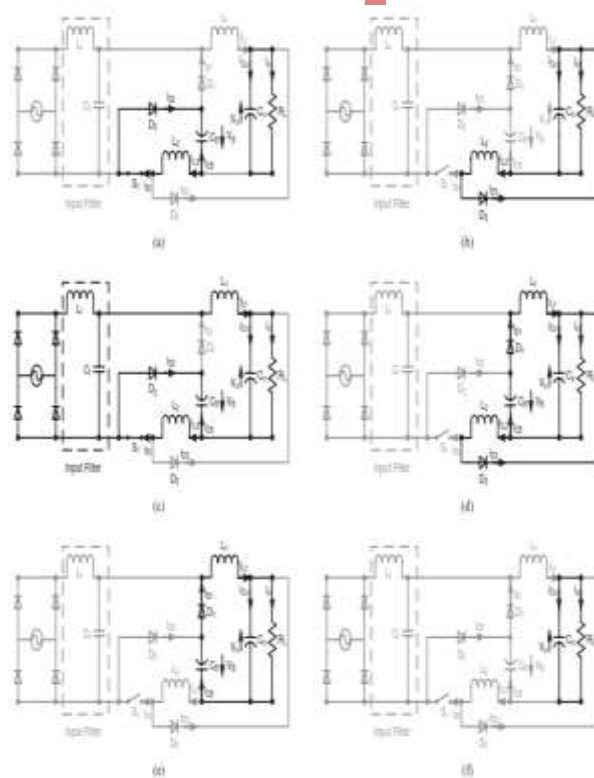


Fig 2: Circuit Operation Stages for dc/dc converter

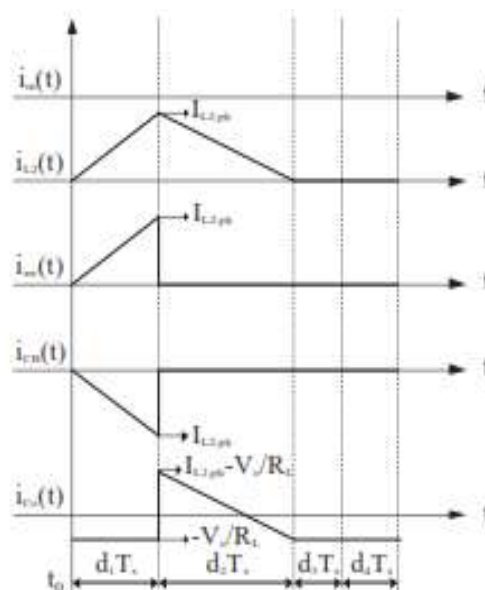


Fig 3 (a) : Key waveform of the proposed circuit

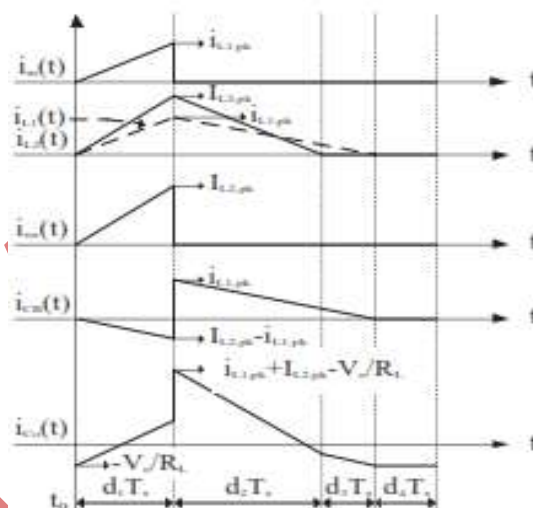


Fig 3(b) : Key waveform of the proposed circuit

III SIMULATION DIAGRAM AND RESULTS

The performance of the proposed circuit is verified by the prototype. To ensure the converter working properly with constant output voltage, a simple voltage mode control is employed. To achieve high performance of the converter for universal line operation in terms of low bus voltage ($< 150\text{V}$) and high power factor ($> 96\%$), the inductance ratio has to be optimized according to Figs. 4 and 5. The lower the bus voltage of the converter, the lower voltage rating capacitor (150 V) can be used. In addition, the inductance ratio will affect the efficiency of the converter. More detail will be given in Section V.

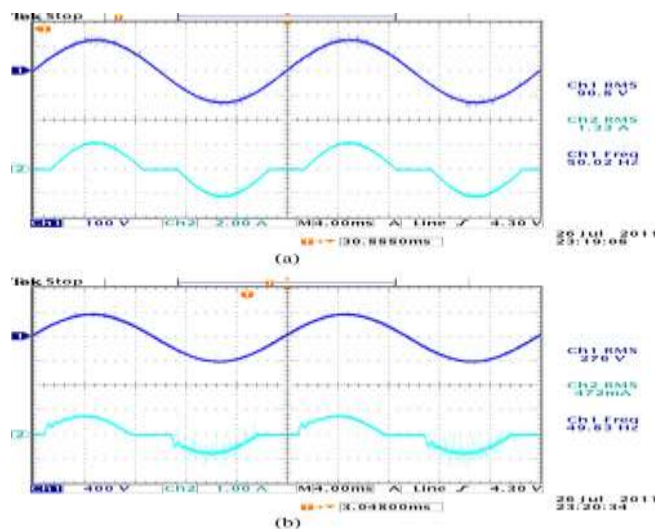


Fig 4: Measurement of input characteristics of the converter

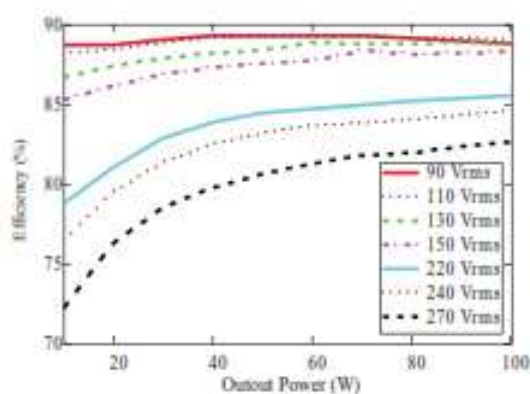


Fig 5: Measured Circuit Efficiency Under Load Variation.

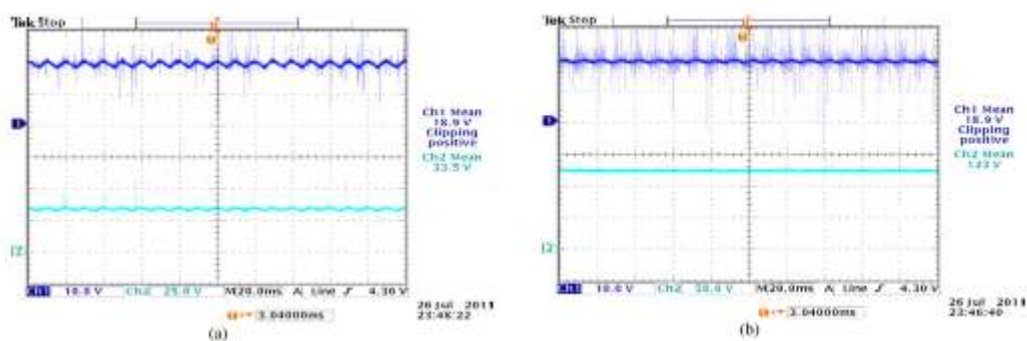


Fig 6: Measured Output Voltage

IV CONCLUSION

The proposed single-stage ac/dc converter has been experimentally verified, and the results have shown good agreements with the predicted values. The intermediate bus voltage of the circuit is able to keep below 150 V at all

input and output conditions, and is lower than that of the most reported converters. Thus, the lower voltage rating of capacitor can be used. Moreover, the topology is able to obtain low output voltage without high step-down transformer. Owing to the absence of transformer, the demagnetizing circuit, the associated circuit dealing with leakage inductance, and the cost of the proposed circuit are reduced compared with the isolated counterparts. In addition, the proposed converter can meet IEC 61000-3-2 standard, and provide both input surge current and output short-circuit protection.

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