

A REVIEW PAPER ON DESIGN AND SIMULATION OF UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER ON FIELD PROGRAMMABLE GATE ARRAY USING VHDL

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ABSTRACT

Universal Asynchronous Receiver Transmitter (UART) is the use of the serial communication protocol, low velocity, short distance, low cost data exchange between computer and peripherals. Due to simultaneous transmission of data bits or multiple accesses, the system complexity increases, in parallel communication so, to alleviate this drawback, we use serial communication. UART includes three modules which are received, the baud rate generator and transmitter. The UART design with Very High Description Language can be integrated into the Field Programmable Gate Array to achieve reliable, compact and stable data transmission.

In the result and simulation part, this project will focus on check the receive data with error free & baud rate generation at different frequencies. The proposed work suggests application design using UART. All modules are designed using VHDL and implemented on Xilinx FPGA development board.

Keywords: VHDL, FPGA, Xilinx ISE.

I. INTRODUCTION

In several control systems, the UART can be widely used for serial communications. A universal asynchronous receiver/transmitter which plays the vital role in serial data transmission. It manages the conversion between parallel and serial data. Serial communication reduces the distortion of a signal, therefore makes data transfer between two systems separated in great distance possible. It contains a parallel to serial converter for data transmitted from the computer and a serial to parallel converter for data coming in via the serial line. The UART also has a buffer for temporarily storing data from high speed transmissions.

The UART serial communication module is divided into three sub modules: the baud rate generator, receiver module and transmitter module. The baud rate generator is used to produce a local clock signal which is much higher than the baud rate to control the UART receive and transmit; The UART receiver module is used to receive

the serial signals at RXD, and convert them into parallel data; The UART transmit module converts the bytes into serial bits according to the frame format and transmits those bits through TXD.

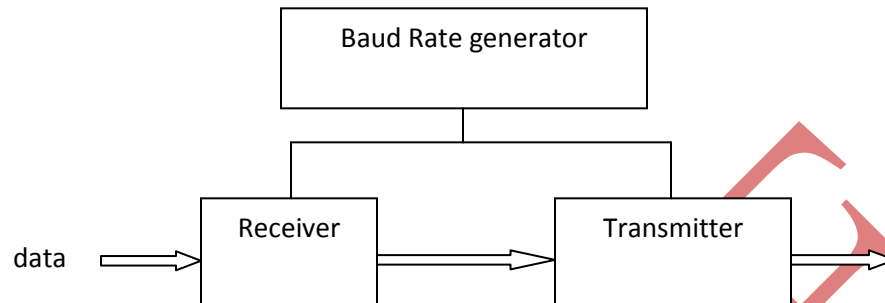


Fig1: UART Module

UART Transmission Protocol:

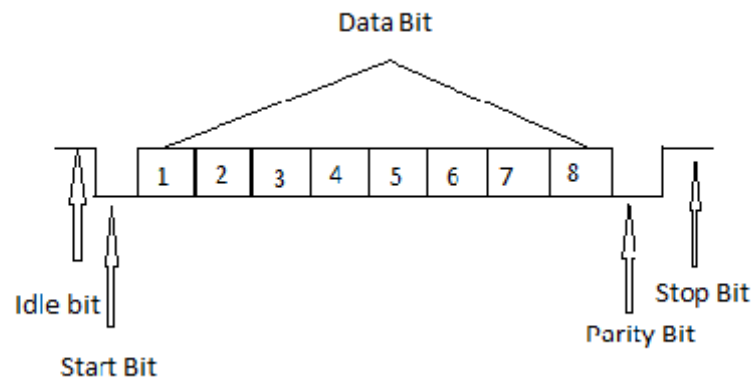


Fig 2: UART Frame Format

It usually includes start bit, data bit, parity bit, stop bit and idle state as shown in fig 2. When a word is given to the UART for Asynchronous transmissions, a bit called the “Start Bit” is added to the beginning of each word that is to be transmitted. The Start Bit is used to alert the receiver that a word of data is about to be sent, and to force the clock in the receiver after the Start Bit, the individual bits of the word of data are sent, with the Least Significant Bit (LSB) being sent first into synchronization with the clock in the transmitter. When the entire data word has been sent, the transmitter may add a Parity Bit that the transmitter generates. The Parity Bit may be used by the receiver to perform simple error checking. Then at least one Stop Bit is sent by the transmitter. If incorrectly formatted data is received, the UART may signal a framing error. If another byte is received before the previous one is read, the UART will signal an overrun error.

II. RELATED WORK

Dr. Garima Bandhawarkar Wakhle et al. suggested that, the UART is the use of the serial communication protocol, which permits the full duplex communication in serial link. They design the hardware implementation of a high speed & competent UART using Field Programmable Gate Array. The UART consists of three components, namely receiver, transmitter & baud rate generator which is also frequency divider. They simulated on Modelsim SE 10.0a and design by using Verilog description language which has been synthesized on FPGA kits like as Spartan3 & Virtex4. After analyzing the comparative analysis conclude that there is a difference in between the number of slices, LUTs and the maximum frequency. The results are quite stable and reliable and have great flexibility with high integration. If we use FIFO in making the UART our design becomes more flexible, stable and reliable which provides highest bps rate. [1]

Amanpreet Kaur, Amandeep Kaur concludes that, A UART is a full duplex receiver and transmitter. It is the chip with programming that controls a computer's an interface to its connected serial devices. It manages the transmission between serial and parallel data. The whole process of serial transmission is operating on the principle of the shift register. In data transmission through the UART, once the baud-rate has been originated, both the transmitter & the receiver's internal clock are set to the identical frequency. [2]

As per Bhavna manure and Rahul tenure is concerned, developing a serial communication protocol including bit synchronization, automatic baud rate detection with selection and bus, frequency division according to the input clock. All modules are simulated on Xilinx Spartan-3 FPGA development board using Verilog programming language and. In the simulation part focus on check the receive data with error free & baud rate generation at various frequencies. The Baud Rate Generator is incorporated into UART design, before the entire design is synthesized. The importance of frequency divider at such places where the user needs lower frequent to operate the functionality. This frequency divider will automatically adjust as per requirement. Observed simulated waveforms at various frequencies between 150 bps to 38400 bps at 50 MHz clock cycles. The simulated waveforms in this prove the consistency of the HDL implementation to describe the architecture and features of the baud rate generator with UART design. [3]

Fang Yi-Yuan Chen Xue-Jun mention that Universal Asynchronous Receiver Transmitter is mainly using for serial communication as well as for low speed, short-distance, low-cost data exchange between computer and its peripherals. The UART designed with VHDL language can be consolidated into the Field Programmable Gate Array to achieve stable, compact & efficient data transmission. It's important for the design of System on Chip. The results of simulation on Quartus II are completely reliable with the UART. In this paper for designing it uses VHDL as a design language to acquire the modules of the UART. The simulation and test part is done by using Quartus II software Altera Cyclone series FPGA chip. The results are reliable & stable, the design has high integration, great flexibility with some reference value. Mainly in electronic designing field, where SOC technology has recently become widely used, this design shows great significance. [4]

From the survey, it is observed that the implementation of UART basically uses the on-chip UART IP hard core because it has high performance, but it has poor flexibility and poor transportability, hence it is usually unable to meet the high requirements of the customer. With the rapid development of FPGA soft core plays an increasingly important role in embedded system, depending on the high performance, high flexibility, transportability and configuration. Huimei Yuan, Junyou Yang and Peipei Pan presented new methodology that provide simple Design of UART IP Soft Core based on DMA Mode. [5]

III.APPLICATIONS

From the reported work it has been observed that researches have proposed various techniques to improve the design techniques of the UART chip. Taking all the advantages and features suggested by different researchers we are defining an application of UART where there is serial communication of keyboard characters from PC hyper terminal through RS232 serial port using UART controller will be display on the HD44780 based 16*2 LCD display using LCD controller. The hardware implementation of UART Controller and LCD driver is based on VHDL language. The proposed block diagram is shown below:

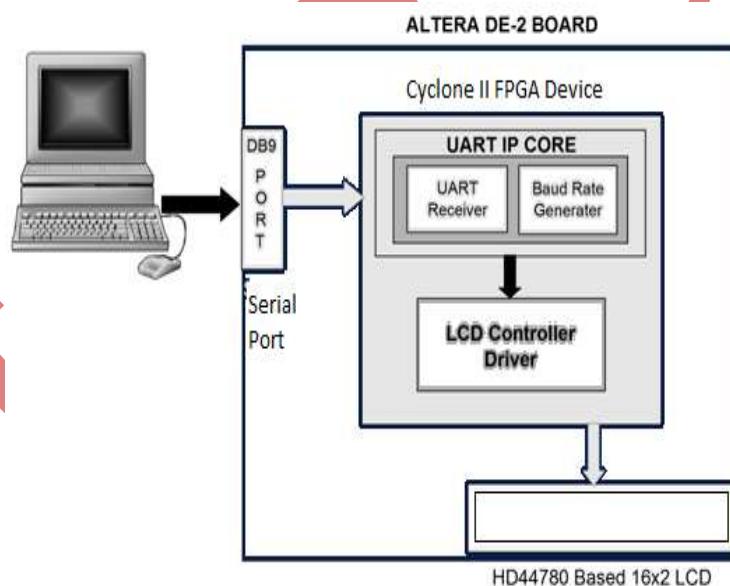


Fig3: Application Design of UART

IV. CONCLUSION

From review of various papers we conclude that this design uses VHDL language to acquire the modules of Universal Asynchronous Receiver Transmitter. Using Xilinx software, FPGA chip to complete simulation and test whose results will be stable and reliable. From this we are designing an application that usage of UART to achieve benefits like greater flexibility, low cost, high performance logic solutions and also meet communication demand quickly and efficiently.

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