DESIGN AND ANALYSIS OF A MULTIPLIER WITH LOW POWER AT .5 SUBMICRON TECHNOLOGY USING TANNER TOOL V12.5 & XILINX 6.1I

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ABSTRACT

A GDI-XOR Based Multiplier has been designed for 3V operation. Multiplication is a fundamental operation in most signals processing algorithms. [1] The multiplier can perform various arithmetic and logical operations. They play a very important role in today's digital circuits. The design of high speed, less delay, low power consumption, less area, and low irregularity in layout are important. For designing an energy efficient processor, a multiplier design decides the digital signal processors efficiency. The basic blocks of a multiplier are adders and AND gate. A multiplier is a digital circuit which performs arithmetic, logic on n-bit digital words.

Keywords: GDI-XOR Based Full Adder, GDI-XOR Based Multipliers, Low Power, Submicron.

I INTRODUCTION

This thesis work focuses on the reduction of the power dissipation, which is showing an ever increasing growth with the scaling down of the technologies. Various techniques at the different levels of the design process have been implemented to reduce the power dissipation at the circuit, architectural and system level [2]. Furthermore, the number of gates per chip area is constantly increasing, while the gate switching energy does not decrease at the same rate, so the power dissipation rises and heat removal becomes more difficult and expensive

Multiplication is one of the basic functions used in digital signal processing. Most high performance DSP systems rely on hardware multiplication to achieve high data throughput. This research uses an approach is based on using low power, having minimal transistor GDI- XOR adders that are the determining in the performance of the multiplier. In this report, we find the delay performance characteristics of conventional and proposed design. We realized conventional multiplier and GDI-XOR based multiplier using conventional adder and GDI-XOR based full adder respectively for better performance.

II GATE DIFFUSION INPUT (GDI)

GDI method is based on the use of a simple cell as shown in figure 1. The design is like an inverter, but the main differences that it Consist of three inputs- G (gate) input to NMOS/PMOS), P (input to source of PMOS)

and N (input to source of NMOS) and Bulks of both NMOS and PMOS are connected to N or P (respectively), so it can be biased with CMOS inverter.

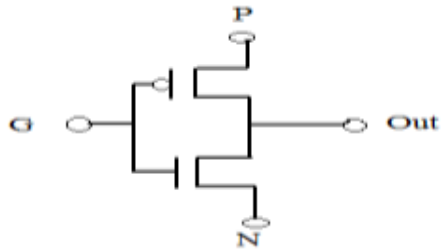


Fig. 1: Basic GDI Cell

Table: 1 Various Logic Functions Of GDI Cell

N	P	G	Out	Function
'0'	B	A	AB	F1
B	'1'	A	A+B	F2
'1'	B	A	A+B	OR
B	'0'	A	AB	AND
C	B	A	AB+AC	MUX

III CMOS Inverter

An inverter or NOT gate is logic gate which invert circuit outputs a voltage representing the opposite logic level to its input. Inverters can be constructed using a single NMOS transistor or a single PMOS transistor coupled with a resistor.

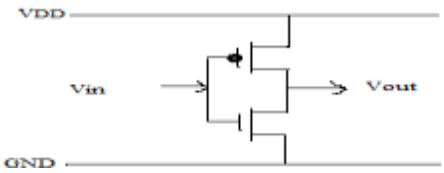
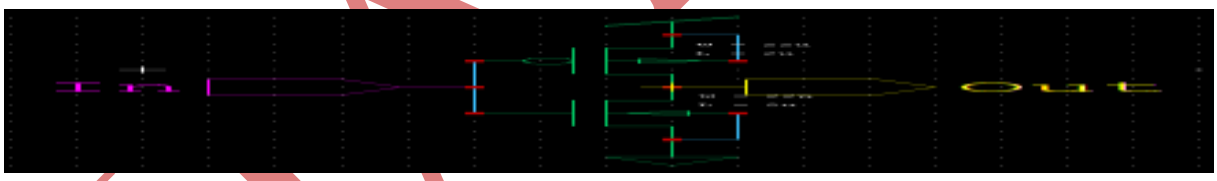


Fig. 2: Block Diagram of Inverter

Table 2: T.T. Of Inverter

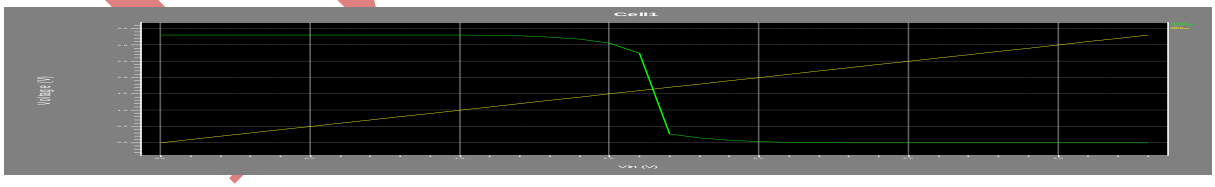
INPUT	OUTPUT
A	NOT A
0	1
1	0

Schematic of Inverter

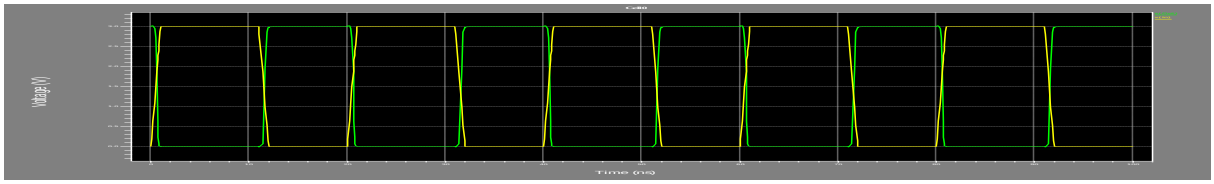


Waveforms:

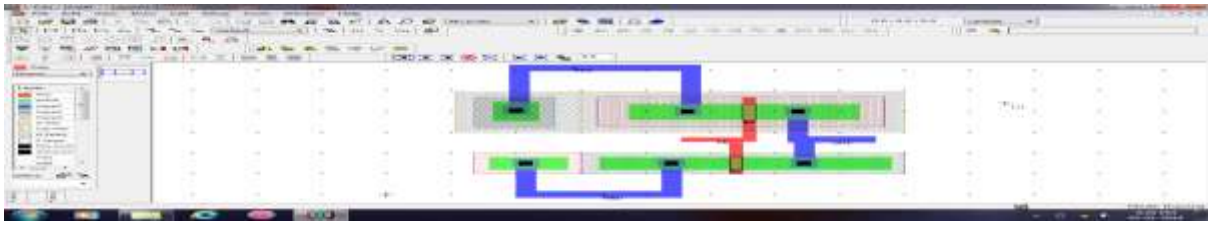
i) DC Analysis



ii) AC Analysis



iii)Layout



IV GDI BASED AND GATE

A two input CMOS AND Gate, the AND function can be obtained with CMOS pairs. PMOS devices are in parallel to provide pull-up configuration and NMOS devices are in series to provide pull-down configuration.

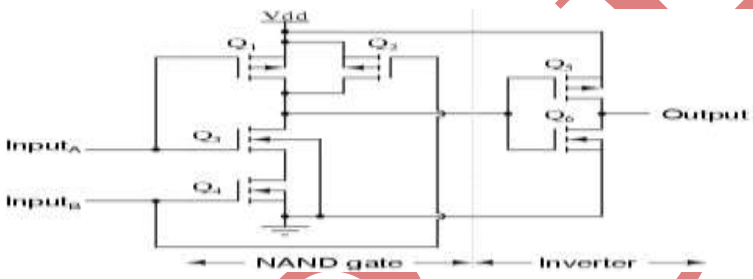
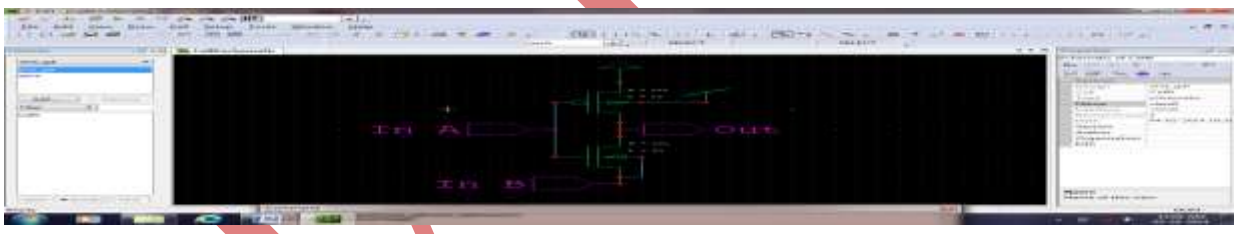


Fig. 3: Block Diagram of AND Gate

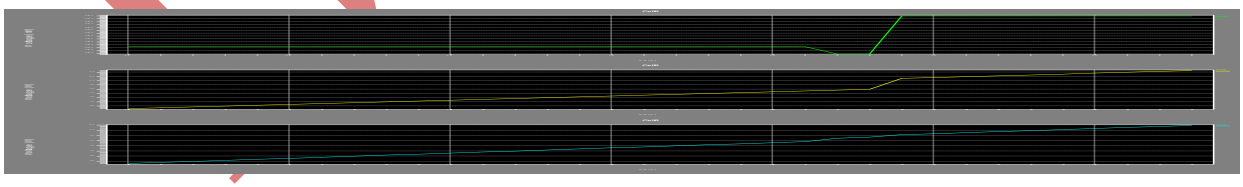
Schematic and waveform (DC and AC Analysis)

Schematic

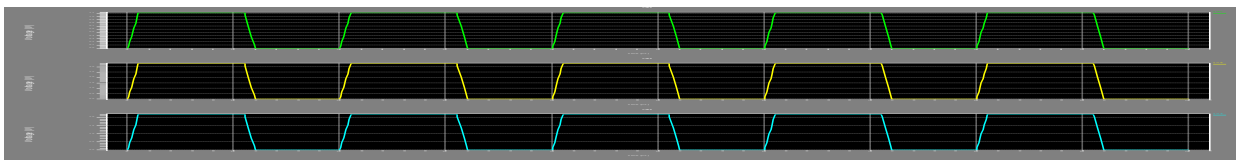


Waveforms

i) DC Analysis



ii) AC Analysis



V ADDER MODULES

Adders are the fundamental building blocks in all the multiplier modules. Fast and efficient full adders play a key role in the performance of the entire system. A full adder could be defined as a combinational circuit that forms the arithmetic sum of three input bits. The Boolean expressions for the SUM and CARRY bits are as shown below.

$$SUM = A \oplus B \oplus Cin$$

$$CARRY = A \cdot B + A \cdot Cin + B \cdot Cin$$

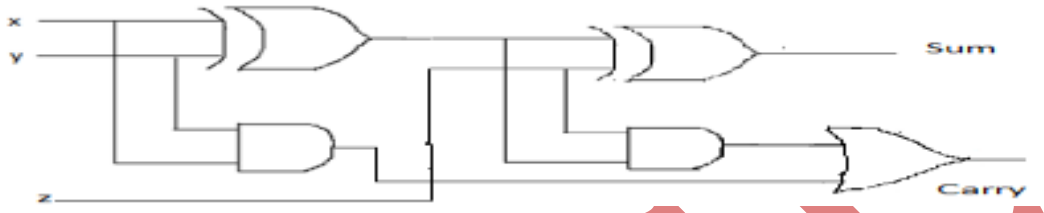
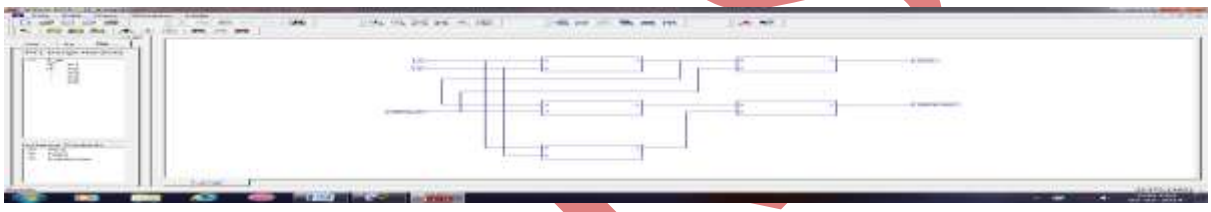


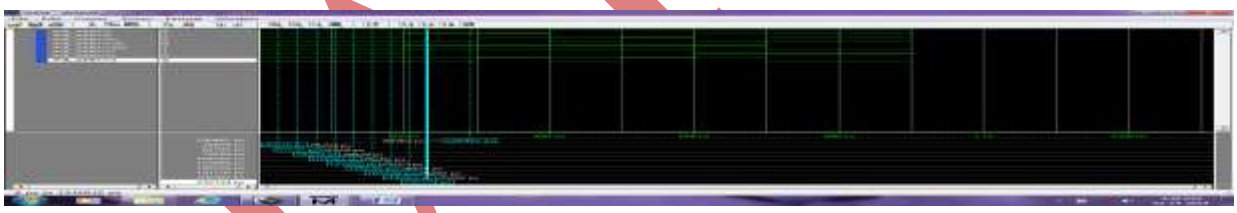
Fig. 4: Block Diagram for Designing of full adder

RTL View and Output Waveform Full Adder:

RTL View



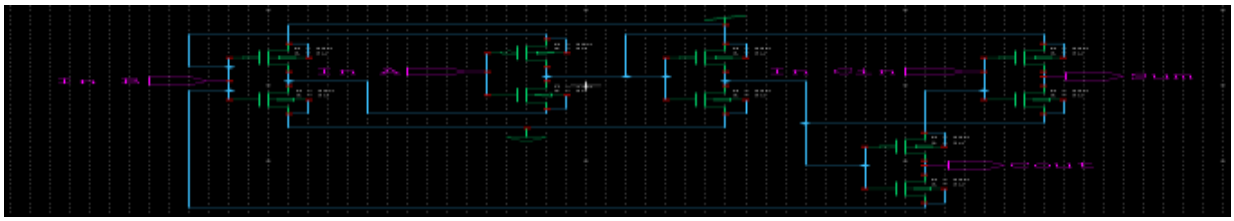
Output waveform using VHDL



Schematic and Waveform (DC And AC Analysis)

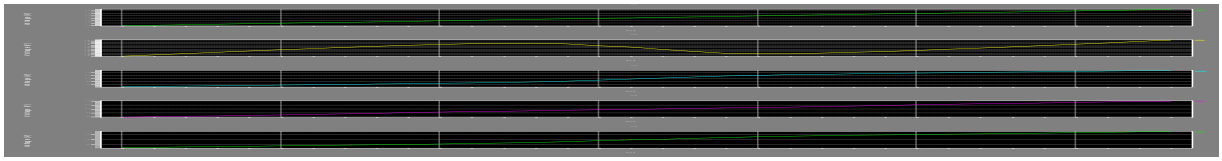
Schematic of Conventional Full Adder

Schematic of GDI Based Full Adder

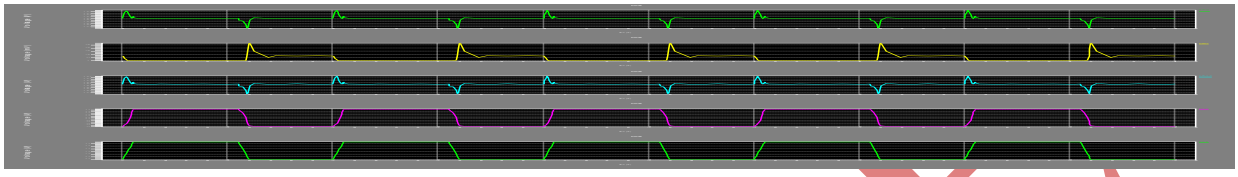


Waveforms

i) DC Analysis



ii) AC Analysis



VI MULTIPLIER

The addition is vital in many applications such as ALUs, multiply-and accumulates (MAC) units in DSPs, and microprocessor [3]. Different multipliers implementation are exists Where as some are good for low power dissipation. In the implementation of digital multipliers binary adders are an essential component [4]. Designing multipliers with low power, energy efficient adders reduce the power consumption and efficiency of multipliers.

6.1 Conventional Multiplier

An array multiplier is very regular in structure. It uses short wires that go from one full adder to adjacent full adders horizontally; vertically test can compute all and terms simultaneously [5]. The terms are summed by an array of 'n [n - 2]' full adders and 'n' no of half adders. The advantage of array multiplier is its regular structure. This reduces the risk of mistakes and also reduces layout design time. This regular layout is widely used in DSP chips. Array Multiplier gives more power consumption as well as optimum number of components required, but delay for this multiplier is larger. It also requires larger number of gates because of which area is also increased; due to this array multiplier is less economical .Thus, it is a fast multiplier but hardware complexity is high.

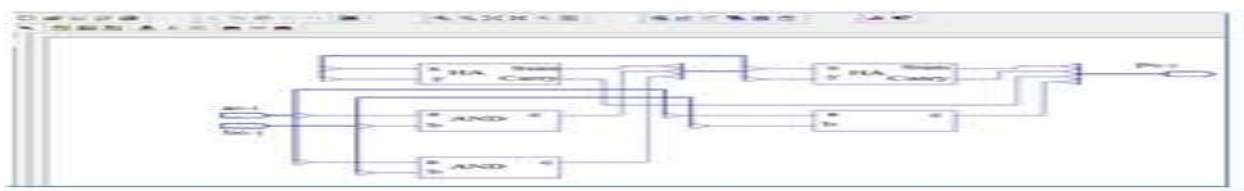
6.2 GDI-XOR Multiplier

In this proposed architecture we are using GDI-XOR full adder and sleepy and gate to design the total architecture with low power dissipation. Here we designed multiplier architectures in array and tree style with these low power components for VLSI and Embedded applications.

VII 7.1 2Bit Multiplier

RTL View and Output Waveform Full Adder

RTL View



Output waveform using VHDL

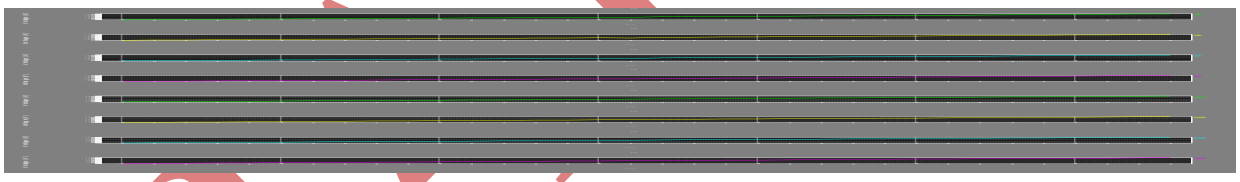
Schematic And Waveform (DC And AC Analysis)

Schematic of Conventional 2Bit Multiplier

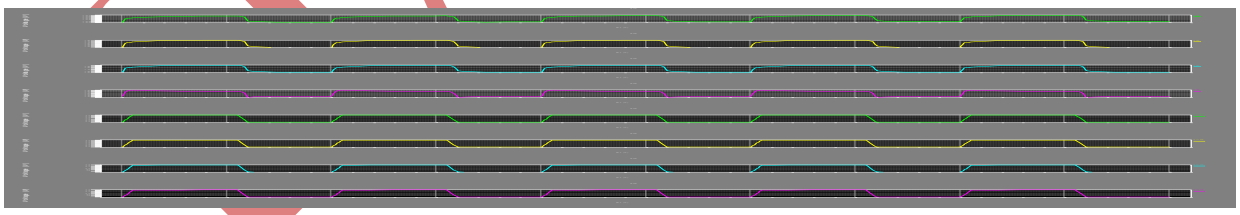
Schematic of GDI Based 2Bit Multiplier

Waveforms

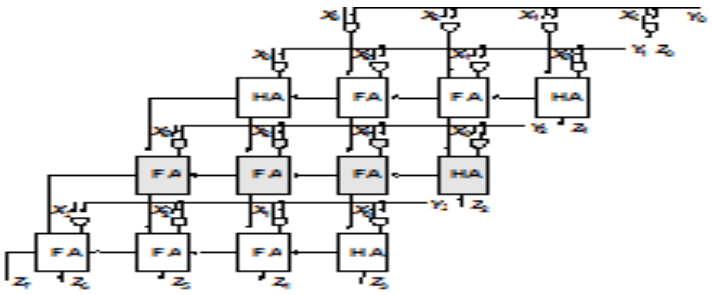
i) DC Analysis



i) AC Analysis



7.2 Block Diagram for Designing of 4 Bit Multipliers



RTL View and waveform of 4 Bit Multipliers

RTL View:

Output waveform using VHDL:

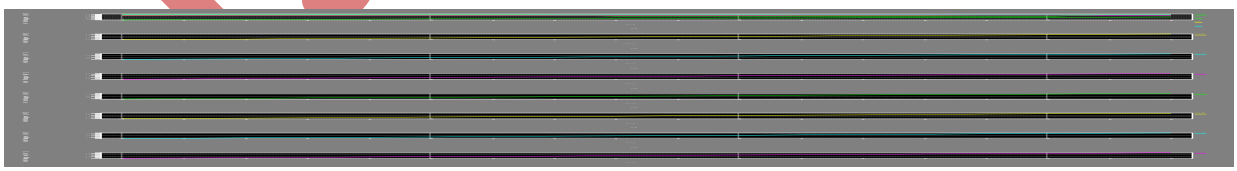
Schematic and waveform (DC and AC Analysis)

Schematic of Conventional 4Bit Multiplier

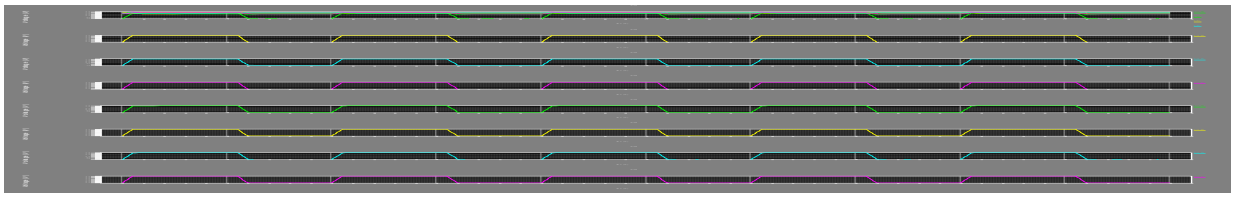
Schematic of GDI Based 4Bit Multiplier

Waveforms

i) DC Analysis

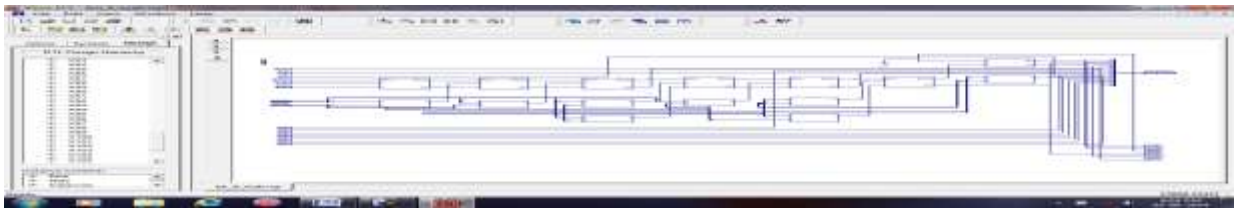


ii) AC Analysis



7.3 RTL View and waveform of 8 Bit Multipliers

RTL View:



Output waveform using VHDL

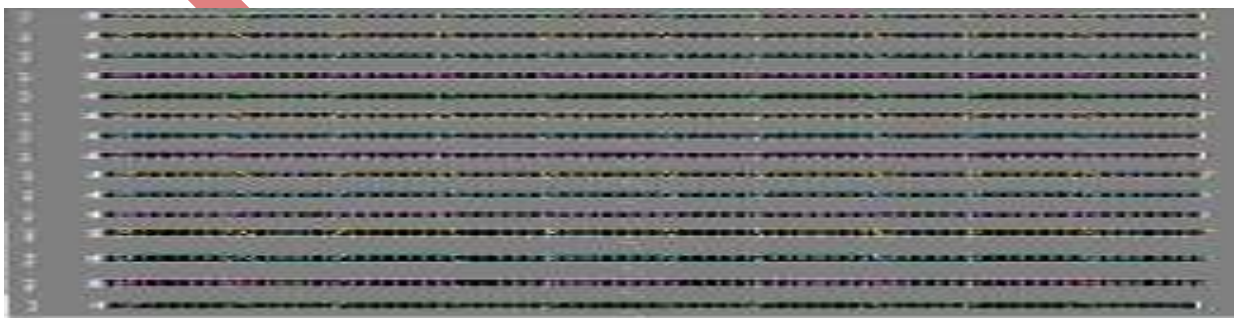
Schematic and waveform (DC and AC Analysis)

Schematic of 8Bit Multiplier:

Waveforms

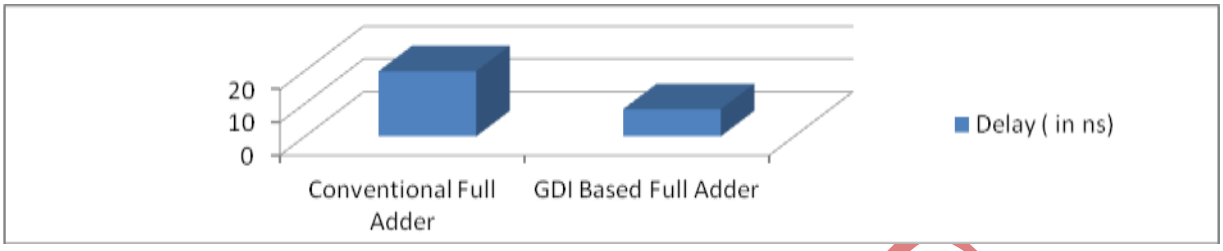
i) DC Analysis:

ii) AC Analysis:



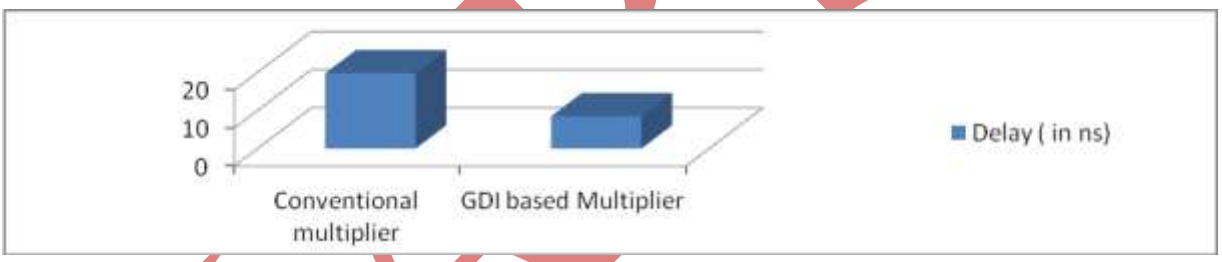
VIII Results

8.1 Comparison of Conventional and GDI based Full Adder



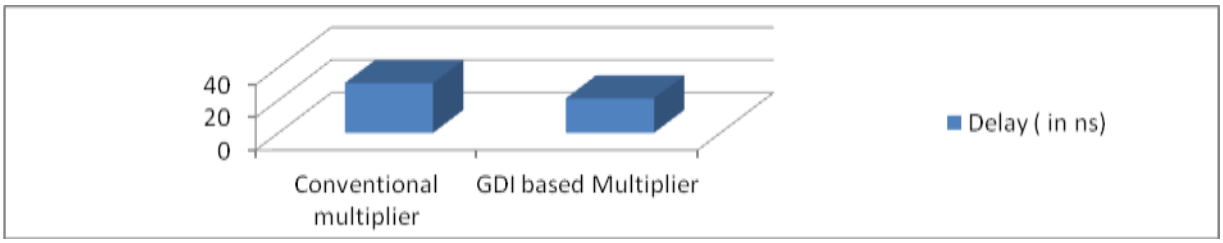
Conventional Full Adder	GDI based Full Adder
Total Delay: 19.805ns	8.234 ns
Total memory: 96550 kilobytes	68956 kilobytes
Total transistor: 28	10

8.2 Comparison of Conventional and GDI based 2Bit Multiplier



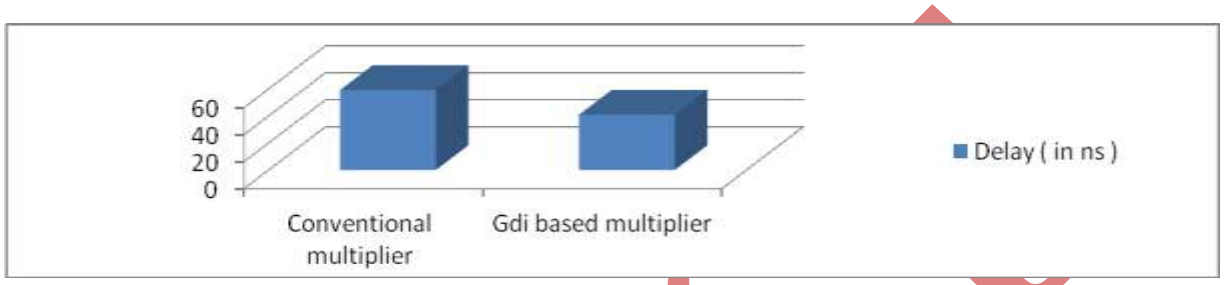
Conventional Multiplier	GDI based Multiplier
Total Delay: 19.805ns	8.468 ns
Total memory: 87680 kilobytes	66168 kilobytes
Total transistor: 52	20

8.3 Comparison of Conventional and GDI Based 4Bit Multiplier



Conventional Multiplier	**GDI based Multiplier**
Total Delay: 30.468 ns	21.068 ns
Total memory: 80590 kilobytes	67960 kilobytes
Total transistor: 528	128

8.4 Comparison of Conventional and GDI based 8 Bit Multiplier



Conventional Multiplier	**GDI based Multiplier**
Total Delay: 59.386ns	41.060ns
Total memory: 67960 kilobytes	190,288 kilobytes
Total transistor: 1892	584

IX CONCLUSION

We evaluate the performance of conventional and modified GDI-XOR multipliers and implement. For Design Entry, we used TANNER TOOS v12.5 and Model Sim6.5c and design with VHDL. In order to get the power report and delay report we synthesize these multipliers using Xilinx ISE 6.1i.The comparison of synthesis report for convention al and modified multipliers. It has been observed that the proposed basic multiplier and GDI-XOR multiplier have less power consumption compared to general one. Here we are placing low power full adder GDI-XNOR full adder to reduce leakage power and we observed that in architectural model tree structural multiplier have less power consumption compared to array structural multiplier.

This newly proposed 4 bit multiplier architecture can be used to design all the low power VLSI and Embedded devices

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