

SECURITY SYSTEM BASED ON VOICE SENSORS

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ABSTRACT

As our project we are going to present "Power Line Communication". Our project mainly used for telecommunication Tele-protection and Tele-monitoring between electrical substations through power lines at high voltages, such as 110kV, 220kV, 400kV. In a PLCC system the communication is established through the power line.

Keywords: LCD, ASCII, PLCC system.

I INTRODUCTION

Power line communication (PLC) is a technique transmitting voice or data at a rapid speed through a power line in a house, an office, a building, and a factory, etc. Power-line communication systems have become increasingly viewed employed as an attractive alternative to conventional hard-wired communication systems, which require dedicated communication wiring, and wireless systems, which involve complex and costly transmitter and receiver circuits. In power line communication, the existing alternating current (AC) power wires serve as a transmission medium by which information is relayed from a transmitter or control station to one or more receivers or loads connected downstream from an AC source. There is a significant advantage to the use of alternating current (AC) power lines for purpose of communication between electronic devices using a power line communication system. Since no new wires are required to implement the function of communication, power-line communication systems greatly reduce the complexity and effort of installation, particularly in building retrofit applications in which it is highly desirable to be able to install an energy control system with little or no alteration of the existing electrical wiring.

II CONSTRUCTION

The components used are:

- | | |
|---------------------------------|--------------|
| • IC UM9121B | • Resistors |
| • IC CM8870 | • Capacitors |
| • IC 74154 | • Relay |
| • IC 7805 Power Regulator | • Diode |
| • IC 741 Op. Amplifier | • LED |
| • IC 7447 Seven Segment Display | • Keypad |

- Laser Torch
- Transformer
- Speaker 0.5W

III BLOCK DIAGRAM

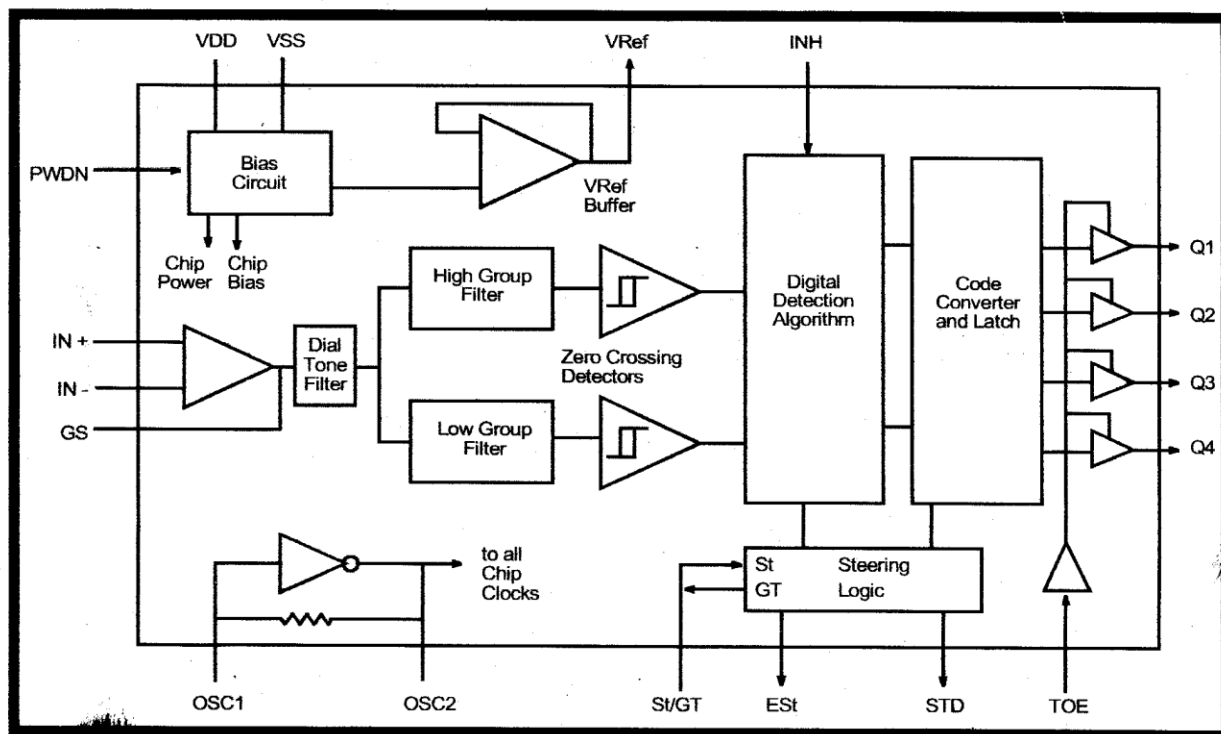
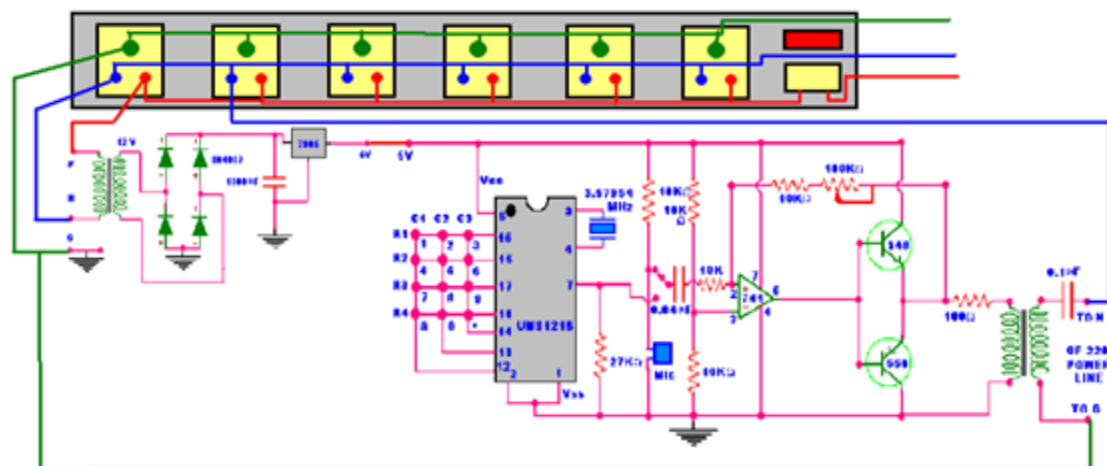


Figure 1 - Functional Block Diagram

IV CIRCUIT DIAGRAM

4.1 Transmitter Section



VI PIN DESCRIPTION

MT8870D/MT8870D-1 ISO²-CMOS

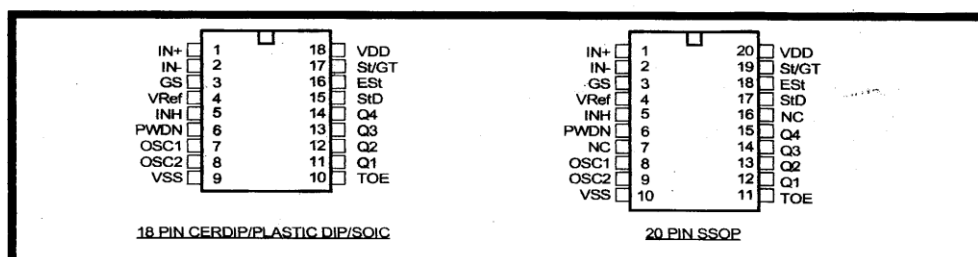


Figure 2 - Pin Connections

Pin Description

Pin #		Name	Description
18	20		
1	1	IN+	Non-Inverting Op-Amp (Input).
2	2	IN-	Inverting Op-Amp (Input).
3	3	GS	Gain Select. Gives access to output of front end differential amplifier for connection of feedback resistor.
4	4	V _{Ref}	Reference Voltage (Output). Nominally V _{DD} /2 is used to bias inputs at mid-rail (see Fig. 6 and Fig. 10).
5	5	INH	Inhibit (Input). Logic high inhibits the detection of tones representing characters A, B, C and D. This pin input is internally pulled down.
6	6	PWDN	Power Down (Input). Active high. Powers down the device and inhibits the oscillator. This pin input is internally pulled down.
7	8	OSC1	Clock (Input).
8	9	OSC2	Clock (Output). A 3.579545 MHz crystal connected between pins OSC1 and OSC2 completes the internal oscillator circuit.
9	10	V _{SS}	Ground (Input). 0V typical.
10	11	TOE	Three State Output Enable (Input). Logic high enables the outputs Q1-Q4. This pin is pulled up internally.
11-14	12-15	Q1-Q4	Three State Data (Output). When enabled by TOE, provide the code corresponding to the last valid tone-pair received (see Table 1). When TOE is logic low, the data outputs are high impedance.
15	17	StD	Delayed Steering (Output). Presents a logic high when a received tone-pair has been registered and the output latch updated; returns to logic low when the voltage on St/GT falls below V _{TSt} .
16	18	ESd	Early Steering (Output). Presents a logic high once the digital algorithm has detected a valid tone pair (signal condition). Any momentary loss of signal condition will cause ESd to return to a logic low.
17	19	St/GT	Steering Input/Guard time (Output) Bidirectional. A voltage greater than V _{TSt} detected at St causes the device to register the detected tone pair and update the output latch. A voltage less than V _{TSt} frees the device to accept a new tone pair. The GT output acts to reset the external steering time-constant; its state is a function of ESd and the voltage on St.
18	20	V _{DD}	Positive power supply (Input). +5V typical.
7, 16		NC	No Connection.

The LCD interface is a parallel bus, allowing simple and fast reading/writing of data to and from the LCD. This waveform will write an ASCII Byte out to the LCD's screen. The ASCII code to be displayed is eight bits long and is sent to the LCD either four or eight bits at a time. If four bit mode is used, two "nibbles" of data (Sent high four bits and then low four bits with an "E" Clock pulse with each nibble) are sent to make up a full eight bit transfer. The "E" Clock is used to initiate the data transfer within the LCD.

Sending parallel data as either four or eight bits are the two primary modes of operation. While there are secondary considerations and modes, deciding how to send the data to the LCD is most critical decision to be made for an LCD interface application. Eight bit mode is best used when speed is required in an application and at least ten I/O pins are available. Four bit mode requires a minimum of six bits. The "R/S" bit is used to select whether data or an instruction is being transferred LCD. If the Bit is set, then the byte at the current LCD "Cursor" Position can be read or written. When the Bit is reset, either an instruction is being sent to the LCD or the execution status of the last instruction is read back (whether or not it has completed). The different instructions available for use with the 44780 are shown in the table below:

VII CONCLUSION

We have presented "Power line Communication" as our project. Our Project mainly used for telecommunication Tele-protection and Tele-monitoring between electrical substations through power lines at high voltages, such as 110kV, 220kV, 400kV. In a PLCC system the communication is established through the power line.

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